BACKPLANE SIGNAL TABLE

Pin #	ROW a	ROW b	ROW c
1	SS14	UTL-E-RXD	SS15
2	SS12	UTL-E-TXD	SS13
3	SS10	TIM-A-CDAC	SS11
4	SS08	UTLRST	SS09

UTL-T-RXD	Utility to timing board asynchronous serial received data.
UTL-T-TXD	Utility to timing board asynchronous serial transmitted data.
UTL-T-SCK	Utility to timing board synchronous clock.
UTL-T-STD	Utility to timing board synchronous transmitted data.

1-2, wherein a command sent from the host computer to the utility board must pass through the

computer interface and timing board -

A communications protocol

of the address field of the WRM instruction is an encoding scheme to indicate the P: (program memory) is to be updated; X:, Y: and ROM data memory can also be accessed.

A hiearchical philosophy has been adopted in partitioning which boards perform which time critical tasks. The most time critical tasks of CCD readout timing and voltage control are performed by the timing board which operates on a time scale of order one microsec. Similarly, the VME or SBus interface board performs time critical tasks limited to data handling on a microsec time scale. The utility

There

Resetting DSPs

A facility exists for resetting the DSPs in a variety of ways. Restting DSP is accomplished simply be bringing its REST* pin low, which causes the DSP on the timing board to read the initializing boot

the same timing. This is useful in mosaic applications where several detector arrays have the same geometry and the timing needs to be done strictly in parallel for all the arrays in the mosaic.There is no limit for the number of clock drivers with the same board address. Similar considerations apply to the number of video processing boards, though only one switch address is