Referring to Fig. 1 and the accompanying timing board circuit schematic, the fiber optic receiver U5 converts optical data from the host computer to electrical signals, the clock recovery chip U7 extracts a clock that is synchronous with the incoming data, the programmable array logic (PAL) device U2 converts the serial data stream into 8-bit wide parallel data, and the byte-wide first-in-first-out (FIFO) memory U28 device holds the data until they are read by the DSP a byte at a time with a RDFIFO command. The jumper block JP4-JP10 is used to select the speed range of the incoming data, and is normally set to 4 MHz for compatability with the host computer interface boards. An LED is installed near the fiber optic components to be lit when the circuit is receiving correct data from the host computer interface board, though a jumper can be removed to disable the LED if its too close to sensitive optical sensors. The DSP polls the Empty Flag line of the FIFO prior to reading its contents,

of the next DSP instruction by a programmable number of clock cycles, according to the scheme -

If D23 = 0 then delay by the ntng t2.ta D22 of 20 nanosec clock cycles.
If D23 = 1 then delay by the ntng t2.ta D22 of 160 nanosec clock cycles.

read over the backplane into the DSP by reading from one of 32 memory mapped locations over the

A watchdog timer and reset circuit U24 is installed to reset the DSP under several conditions. The DSP will be reset whenever the on-board push button S1 is depressed. The DSP will be reset if the +5volts digital power line crosses below 4.75 volts,

3	H3	HVEN	Either	High voltage enable, low true
4	H4	STATUS0	Either	General use - backplane A25
5	H5	STATUS1	Either	General use - backplane A26
6	H6	STATUS2	Either	General use - backplane A27
7	H7	STATUS3	Either	General use - backplane A28
8	HA0	AUX1	Either	not used
9	HA1	EF*	Input	FIFO Empty flag, low true
10	HA2	FD15	Output	Force D15 to this value if FMODE = 1
11	HR/W	SYNC	Either	Master/Slave sync bit
12	HEN*	FMODE	Output	Forced D15 mode if =1
13	HREQ*	PWRST	Either	Reset power board, low true
14	HACK*	AUX2	Either	not used

The power control board lines LVEN (low voltage enable, to turn on +/- 6.5 and +/- 16.5 volts supplies to the backplane), HVEN (high voltage enable, to turn on the +36 volts supply) and PWRST (turn off all supplies) are programmed as

application in DSP P: memory, typically 256 words -

P: $200 + APL_LEN words, typically 768 words.
Y:

board of the specified type can be set to the 12-bit value.