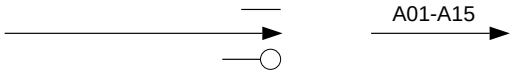
DSP56002



32K X 24

SRAM

ADDRESS

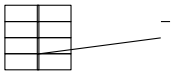
DECODE

DATA BUS
D00-D23

the bus.

WRAM	X:$FFB0	Write address modifiers AM0-AM5, and VME control signals WRITE/I and LWORD/I to a latch for assertion during VMEbus bus master cycles. D0-D5 = AM0-AM5, D6 = WRITE/I, D7 = LWORD/I and D16-D23 = interrupt vector.
RDFIFO	X:$FFB1	Read 18-bit word from the FIFO. It contains image or command/reply data from the timing board.
WRHADR	X:$FFB2	Write the high VME address bits A16-A31 to latches for assertion onto the VMEbus on the next VMEbus master cycle.
WRHDATA	X:$FFB3	Write the DSP data lines D0-D15 on latches for assertion onto the VMEbus data lines D16-D31 on the next bus master cycle if a 32-bit data transaction has been requested by sending the WORD-LENGTH bit of the DSP port B to 32-bit size.
RDCOM		

Bit #	Name	I/O	Function



Jumper Settings

There are many jumpers on the board to select operating modes and addresses. The default settings are as follows -

Command address = $1a000000
Reset address = command address + 4
Fiber optic speed = 50 MHz
Address modifiers = $
Interrupt level = 7
Bus request level = 3
ROM = write disabled EEPROM
Watch dog timer = disabled

Generation II = selected

The figure shows the schematics of the jumper blocks with the default jumper settings. The command address is determined by

```
REP     #20                     ; Wait for the last pixel transmission
NOP
BSET    #FD15,X:PBD             ; Force D15 = 1
MOVEP   #0,Y:WRFO               ; Transmit D0 = 0 to the VME board
BCLR    #FD15,X:PBD             ; Force D15 = 0
REP     #10                     ; Wait for the last pixel transmission
NOP
```

and possibly put the timing board in non-forced data bit D15 mode if images are not to be transmitted continuously -

```
BCLR    #FMODE,X:PBD            ; Take the board out of forced bit mode
```

Application commands

The DSP software chapter describes the commands that are located in the "vmeboot" program that is loaded from EEPROM after the DSP is reset, and are in common with the other DSP boards in the system. These are the read and write memory commands (RDM and WRM), the test data link command (TDL) and the load application command (LDA). Every command to the interface board is prefaced with a header word, consisting of 15 header wordTj 38.581 0 Td (Every)Tj vmeboot" 9 crds in the

downloaded from the host computer or loaded from on-board ROM memory with the command ’LDA 1’. The number of pixels to be read is stored in the DSP memory location Y:1. However, if the number of pixels to be read exceeds the 24-bit range of the DSP data values (16 Mpixels) then the number of columns to be read can be written to Y:2 and the number of rows to Y:3, with the product of the two numbers being calculated ber,