Cyclone III FPGA Starter Board

Reference Manual

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Contents

About this Manual

Revision History

The table below displays the revision history for the chapters in this reference manual.

Chapter	Date	Version	Changes Made
1	April 2007	1.0.0	• First publication.

This reference manual provides comprehensive information about the Altera® Cyclone® III family of devices and the Cyclone III FPGA starter board.

How to Contact Altera

For the most up-to-date information about Altera® products, refer to the following table.

Information Type	Contact *Note (1)*
Technical support	www.altera.com/mysupport/
Technical training	www.altera.com/training/
Technical training services	custrain@altera.com
Product literature	www.altera.com/literature
Product literature services	literature@altera.com
FTP site	ftp.altera.com

Note to table:
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input.` Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or the user's work.
	A warning calls attention to a condition or possible situation that can cause injury to the user.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

1. Introduction

General Description

The Cyclone® III starter board provides a hardware platform that offers a unique opportunity to customize your development environment via expansion connectors and daughter cards as well as evaluate the feature-rich, low-power Altera® Cyclone III device.

For more functionality, the starter board can be expanded through daughter cards connected to the Altera High Speed Mezzanine Card (HSMC) connector. Altera and development kit partners are creating HSMC daughter cards that allow you to expand the functionality of the board.

For the latest information about available HMSC daughter cards, go to **www.altera.com/products/devkits/kit-index.html**.

The main features of the Cyclone III starter board are:

- Low-power consumption Altera Cyclone III EP3C25 chip in a 324-pin FineLine BGA (FBGA) package
- Expandable through HSMC connector
- 32-Mbyte DDR SDRAM
- 16-Mbyte parallel flash device for configuration and storage
- 1 Mbyte high-speed SSRAM memory
- Four user push-button switches
- Four user LEDs

The main advantages of the Cyclone III starter board are:

- Facilitates a fast and successful FPGA design experience with helpful example designs and demonstrations.
- Directly configure and communicate with the Cyclone III device via the on-board USB-Blaster™ circuitry and JTAG header
- Active Parallel flash configuration
- Low power consumption
- Cost-effective modular design

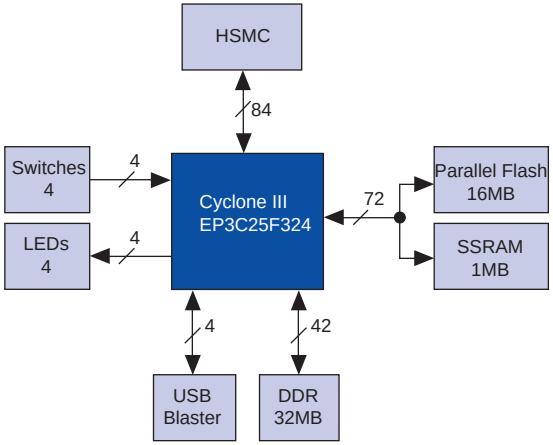
Board Component Blocks

- Altera Cyclone III EP3C25F324 FPGA
  - 25K logic elements (LEs)
  - 66 M9K memory blocks (0.6 Mbits)
  - 16 18x18 multiplier blocks
  - Four PLLs
  - 214 I/Os
- Clock management system
  - One 50 MHz clock oscillator to support a variety of protocols
  - The Cyclone III device distributes the following clocks from its on-board PLLs:
    - DDR clock
    - SSRAM clock
    - Flash clock
- HSMC connector
  - Provides 12 V and 3.3 V interface for installed daughter cards
  - Provides up to 84 I/O pins for communicating with HSMC daughter cards
- General user-interface
  - Four user LEDs
  - Two board-specific LEDs
  - Push-buttons:
    - System reset
    - User reset
    - Four general user push-buttons
- Memory subsystem
  - Synchronous SRAM device
    - 1-Mbyte standard synchronous SRAM
    - 167-MHz
    - Shares bus with parallel flash device
  - Parallel flash device
    - 16-Mbyte device for active parallel configuration and storage
    - Shares bus with SRAM device
  - DDR SDRAM device
    - 56-pin, 32-Mbyte DDR SDRAM
    - 167-MHz
    - Connected to FPGA via dedicated 16-bit bus
- Built-in USB-Blaster interface
  - Using the Altera EPM3128A CPLD
  - For external configuration of Cyclone III device
  - For system debugging using the SignalTap® and Nios® debugging console
  - Communications port for Board Diagnostic graphical user interface (GUI)

Block Diagram

Figure 1–1 shows a functional block diagram of the Cyclone III FPGA starter board.

Figure 1–1. Cyclone III FPGA Starter Board



Handling the Board

When handling the board, it is important to observe the following precaution:

CAUTION

Static Discharge Precaution—Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

2. Board Components & Interfaces

Board Overview

This chapter provides operational and connectivity detail for the board's major components and interfaces and is divided into the following major blocks:

- Featured device
- Clocking circuitry
- Jumpers
- Interfaces
  - USB interface
  - Altera® HSMC expansion connector
  - General user interfaces
- Memory
- Power supply
- Statement of China-RoHS compliance

Board schematics, the physical layout database, and manufacturing files for the Cyclone® III FPGA starter board are included in the Cyclone III FPGA Starter Kit in the following directory:

*<install path>***CycloneIII_Starter_Kit-v7.1.0****BoardDesignFiles**

For information on powering-up the Cyclone III FPGA starter board and installing the demo software, refer to the *Cyclone III FPGA Starter Kit Getting Started User Guide.*

Figure 2–1 shows the top view of the Cyclone III FPGA starter board.

Figure 2–1. Top View of the Cyclone III FPGA Starter Board

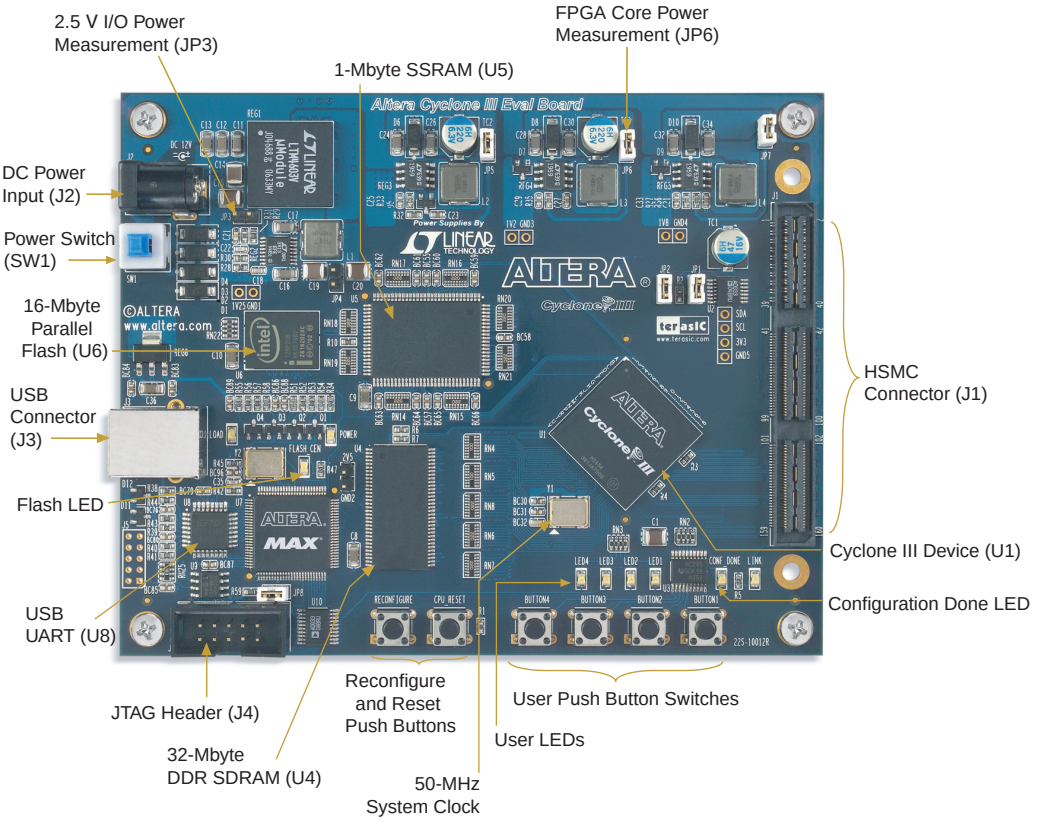


Figure 2–2 shows the diagonal view of the Cyclone III FPGA starter board.

Figure 2–2. Diagonal View of the Cyclone III FPGA Starter Board

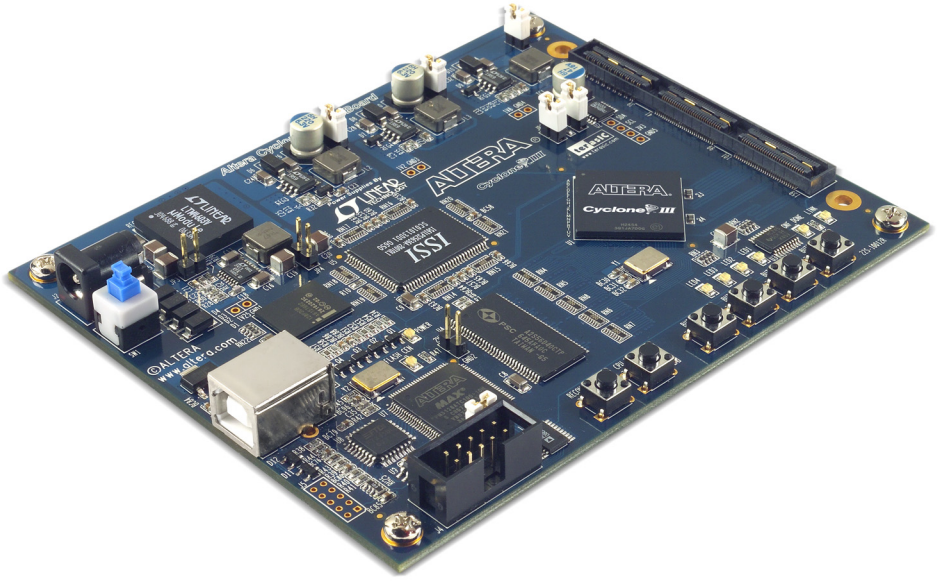


Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Cyclone III FPGA Starter Board (Part 1 of 2)

Type	Component/ Interface	Board Reference	Description	Page
Featured Device				
FPGA	Cyclone III device	U1	EP3C25F324-C8, 324-pin FineLine BGA (FBGA) package	2–5
User Interfaces				
I/O	Push-button switches	Button1–Button4, CPU Reset, Reconfigure	Four push-button switches for user-defined, logic inputs.	2–13
I/O	LEDs	LED1–LED4, Conf_Done, Link, Power, Flash_CEN, Load	Four user-defined LEDs	2–14
Connections & Interfaces				
I/O	USB UART	U8	USB interface to the Cyclone III device for external FPGA configuration and communication with applications running on the FPGA.	2–8
Input	HSMC Connector	J1	Header for connecting the HSMC interface.	2–9
Configuration & Reset				
Input	JTAG header	J4	Jumper header to select which JTAG source the board uses, i.e., the JTAG header configuration or the USB JTAG configuration.	2–8
Input	USB connector	J3	Type B USB Connector that allows for connecting a Type A-B USB cable between a PC and the board.	2–8
Display	Configuration done LED	Conf_Done	LED that illuminates when FPGA is successfully configured.	2–14
Memory				
Flash	16 Mbytes of parallel flash memory	U6	16 Mbytes of non-volatile memory.	2–16
Display	Flash LED		LED that illuminates when the flash is being accessed.	N/A
SSRAM	1 Mbyte high-speed SSRAM	U5	256K x 32 synchronous SRAM	2–20
DDR SDRAM	32-Mbyte DDR SDRAM	U4	4M x16 x 4 DDR SDRAM	2–18

Table 2–1. Cyclone III FPGA Starter Board (Part 2 of 2)

Type	Component/ Interface	Board Reference	Description	Page
Clock Circuitry				
Oscillator	Clock	Y1	50-MHz clock oscillator used for the system clock.	2–6
Power Supply				
Input	DC power jack	J2	12-V DC unregulated power source.	2–22
Input	Power switch	SW1	Switches the board's power on and off.	2–22
Probe point	Current sense resistor	JP6	Measure FPGA core power using current sense resistor.	N/A
Probe point	Current sense resistor	JP3	Measure 2.5 V I/O power (shared between devices) using current sense resistor.	N/A

Featured Device

The Cyclone III FPGA Starter Kit features the EP3C25F324 device (U1) in a 324-pin FineLine BGA (FBGA) package. Table 2–2 lists Cyclone III device features.

Table 2–2. Cyclone III Device Features

Architectural Feature	Results
Altera's third-generation of low-cost FPGAs	• Lowest overall FPGA system cost available • Staggered I/O ring to decrease die area • Wide range of low-cost packages • Support for low-cost serial and parallel flash for configuration options
Lowest power consumption FPGA available	• Based on the TSMC's low-power 65nm process • Supports hot-socketing • Unused I/O banks can be powered down • Extends battery life for portable or hand-held applications • Eliminates or reduces cooling system costs
Increased system integration	• Densities up to 119,088 logic elements • High memory-to-logic ratio • Highest multiplier-to-logic ratio in the industry • Up to four dynamically reconfigurable, cascadable phase-locked-loops (PLLs), each with up to five outputs • Multi-value on-chip termination (OCT) support with calibration feature.

Table 2–3 lists the Cyclone III EP3C25F324 device pin count.

Table 2–3. Cyclone III Device Pin Count

Board Component	Pins
SRAM/flash (shared bus)	72
SDRAM (DDR)	42
Push buttons	4
LEDs	4
USB-Blaster/configuration	4
HSMC	84
Total Pins Used	210
Total EP3C25F324 pins	214
Unused pins	4 *(1)*

Note to Table 2–3:

(1) In some DDR designs, you will be unable to use some of the other I/Os that share the same VREF banks with the DDR. Therefore, if you have added DDR to your system, you will need to remove two or three LEDs or I/Os for the HSMC connector, which shares the same VREF bank as the DDR.

You can configure the Cyclone III device via the on-board USB-Blaster™ or through the JTAG interface using an external programming cable (sold separately).

For additional information about Altera devices, go to **www.altera.com/products/devices**.

Clocking Circuitry

The Cyclone III FPGA starter board's clocking circuitry is designed to be simple and easy to use. A single 50-MHz clock input is used and all other clocks are generated using the Cyclone III device's phase-locked loops (PLLs). The dedicated PLLs are used to distribute the flash, SSRAM, and HSMC clocks.

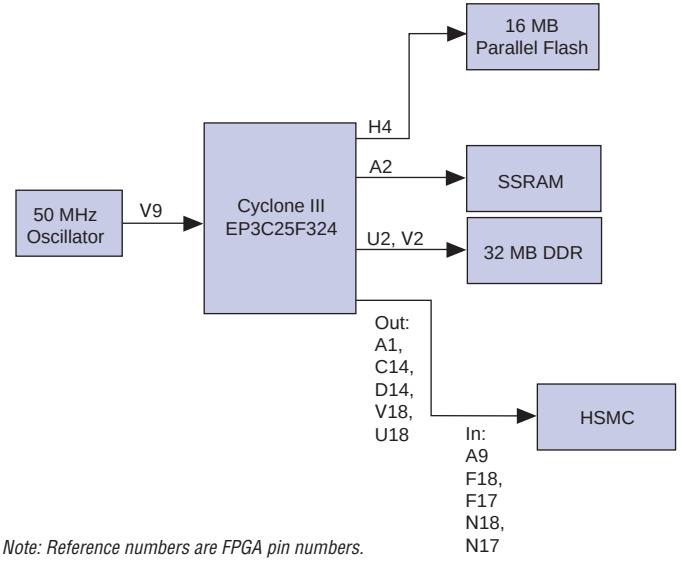
Table 2–4 shows the clock pinout.

Table 2–4. Clock Pinout

Signal Name	FPGA Pin	Direction	Type
50MHz	B9	Input	2.5 V

Figure 2–3 shows the simplest clocking scheme with a single clock input; however, much more complex clocking schemes can be implemented with Cyclone III FPGAs.

Figure 2–3. Cyclone III FPGA Starter Board's Clocking Scheme



Note: Reference numbers are FPGA pin numbers.

Jumpers

Table 2–5 lists board jumpers and jumper operational descriptions.

Table 2–5. Board Jumpers (Part 1 of 2)

Jumper Board Reference	Jumper Operational Descriptions
JP1 and JP2	Removing ***both*** shunts adds the HSMC connector to the JTAG chain. If the shunts are in place on both jumpers, then the HSMC connector is removed from the JTAG chain.
JP3	Sense resistor for measuring the power consumed by the 2.5 V supply to V_{CCIO}, the DDR, the flash I/O, and the SSRAM.
JP4	1.25 V termination supply for DDR2. To supply an external voltage, remove the jumper and connect the external supply to pin 2. (Pin 2 has a rounded shape on the bottom of the board.)

Table 2–5. Board Jumpers (Part 2 of 2)

Jumper Board Reference	Jumper Operational Descriptions
JP5	3.3 V supply for the MAX device and HSMC. To supply an external voltage, remove the jumper and connect the external supply to pin 2. (Pin 2 has a rounded shape on the bottom of the board.)
JP6	Sense resistor for measuring the power consumed by the 1.2 V V_{CCINT} supply to the Cyclone III device.
JP7	1.8 V power supply to flash device. To supply an external voltage, remove the jumper and connect the external supply to pin 2. (Pin 2 has a rounded shape on the bottom of the board.)
JP8	Removing the shunt enables configuration of the Cyclone III device using the JTAG header and an external USB-Blaster. When the shunt is in place, the embedded USB-Blaster circuitry must be used to configure the Cyclone III device. (The board ships without the JTAG header populated.)

Interfaces

This section describes the following Cyclone III FPGA starter board's interface blocks:

- USB interface
- HSMC expansion connector
- General user interfaces

USB Interface

The USB-Blaster circuitry is built onto the board. You can simply plug the USB cable (provided with the kit) into USB connector J3 on the board and the other end to a USB port on your computer to program and communicate with the Cyclone III device via the JTAG port.

A USB physical connection is used to enable computers to communicate with the starter board. To simplify the USB interface, the board contains a FTDI FT2232L USB universal asynchronous receiver/transmitter (UART) circuit. The data from the FTDI chip is translated into a JTAG stream using the Altera EMP3128A CPLD connected to the Cyclone III device's dedicated JTAG port.

The 5 V supply for the FTDI device is drawn from the USB connection. The rest of the circuit operates on 3.3 V supply with 100 mA maximum and 1.8 V supply with 900 mA maximum voltage.

HSMC Expansion Connector

The board provides one HSMC connector. The HSMC connector is a modified version of standard high-speed Samtec connectors. To provide better signal integrity between host boards and daughter cards when using high-speed transceivers, the standard high-speed Samtec connector is modified by removing every third pin in bank -1.

CMOS utilization of the HSMC pins is assumed and no options for supporting other differential signaling is provided with the board. The eight clock-data-recovery high-speed transceiver channels are not connected.

Table 2–6 lists the ordering codes and shows the relationship between the standard Samtec Q-series connectors and the modified parts' ordering codes.

Table 2–6. Altera-Specific & Standard Samtec Part Numbers

	Altera-Specific Samtec Part Number	Standard Samtec Part Number
Daughter cards	ASP-122952-01	QTH-090-01-L-D-A
Host boards	ASP-122953-01	QTH-090-01-L-D-A

The board provides both 12 V unregulated and 3.3 V regulated power supply to the HSMC connector for any installed daughter cards.

For more information regarding the HSMC, refer to the *High Speed Mezzanine Card Electrical and Mechanical Specification* version 1.2 or later.

Table 2–7 lists the guaranteed minimum on-board power supply levels. The power rails are delivered via designated pins on the HSMC connector.

Table 2–7. HSMC Power Requirements

Voltage	Current Rating	Maximum Voltage
12 V	1.0 A	12.0 W
3.3 V	2.0 A	6.6 W

Table 2–8 lists HSMC A connector board reference and manufacturing information.

Table 2–8. HSMC A Connector Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number
J1	High speed Mezzanine card connector	Samtec	ASP-12953-01

The HSMC uses the Samtec connector's header provided on the board. Figure 2–4 shows the outline of the Samtec header.

Figure 2–4. Samtec Connector's Header

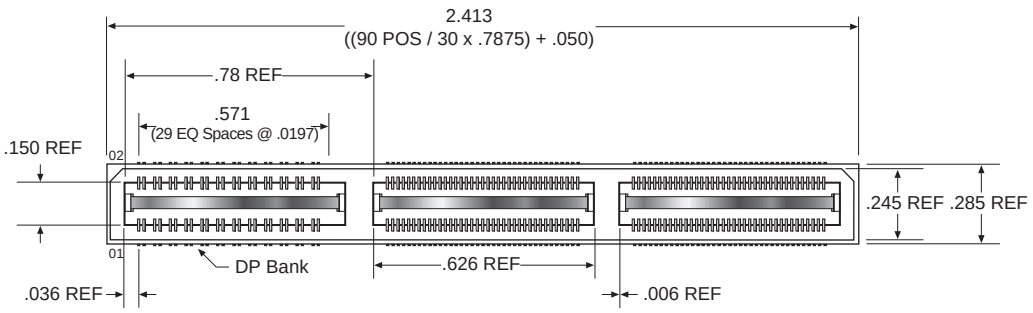


Table 2–9 lists the HSMC Port A interface pins. Signal names and directions are relative to the Cyclone III FPGA. (The HSMC is operating as the host.)

General User Interfaces

To allow you to fully leverage the I/O capabilities of the Cyclone III device, the following are available on the board (remaining I/Os are connected to additional board resources):

- Push buttons: System and user reset, and user-defined push buttons
- LEDs: Board-specific and user-defined LEDs

Some of the board's buttons and LEDs have a specific board function while others are user-defined and are provided to control FPGA designs.

Table 2–9. HSMC Pinout (Part 1 of 3)

Signal Name	FPGA Pin Name	Direction	Type	HSMC Pin
HSMC_SDA	E1	Bidirectional	2.5 V	33
HSMC_SCL	F3	Bidirectional	2.5 V	34
HSMC_TCK	J1			35
HSMC_TMS	J2			36
HSMC_TDI	J6			37
HSMC_TDO	J5			38
HSMC_CLKOUT0	A1	Output	2.5 V	39
HSMC_CLKIN0	A9	Input	2.5 V	40
HSMC_CLKOUT_p1	D14	Output	2.5 V	95
HSMC_CLKIN_p1	F17	Input	2.5 V	96
HSMC_CLKOUT_n1	C14	Output	2.5 V	97
HSMC_CLKIN_n1	F18	Input	2.5 V	98
HSMC_CLKOUT_p2	U18	Output	2.5 V	155
HSMC_CLKIN_p2	N17	Input	2.5 V	156
HSMC_CLKOUT_n2	V18	Output	2.5 V	157
HSMC_CLKIN_n2	N18	Input	2.5 V	158
HSMC_D0	H6	Bidirectional	2.5 V	41
HSMC_D1	D3	Bidirectional	2.5 V	42
HSMC_D2	M5	Bidirectional	2.5 V	43
HSMC_D3	L6	Bidirectional	2.5 V	44
HSMC_D4	M5	Bidirectional	2.5 V	47
HSMC_D5	M3	Bidirectional	2.5 V	48
HSMC_D6	N7	Bidirectional	2.5 V	49
HSMC_D7	T2	Bidirectional	2.5 V	50
HSMC_D8	N8	Bidirectional	2.5 V	53
HSMC_D9	H15	Bidirectional	2.5 V	54
HSMC_D10	J13	Bidirectional	2.5 V	55
HSMC_D11	H16	Bidirectional	2.5 V	56
HSMC_D12	N10	Bidirectional	2.5 V	59
HSMC_D13	N16	Bidirectional	2.5 V	60
HSMC_D14	N11	Bidirectional	2.5 V	61
HSMC_D15	N15	Bidirectional	2.5 V	62
HSMC_D16	K17	Bidirectional	2.5 V	65
HSMC_D17	R16	Bidirectional	2.5 V	66

Table 2–9. HSMC Pinout (Part 2 of 3)

Signal Name	FPGA Pin Name	Direction	Type	HSMC Pin
HSMC_D18	P11	Bidirectional	2.5 V	67
HSMC_D19	T16	Bidirectional	2.5 V	68
HSMC_TX_p4	B2	Bidirectional	2.5 V	71
HSMC_RX_p4	C2	Bidirectional	2.5 V	72
HSMC_TX_n4	B1	Bidirectional	2.5 V	73
HSMC_RX_n4	C1	Bidirectional	2.5 V	74
HSMC_TX_p5	G2	Bidirectional	2.5 V	77
HSMC_RX_p5	H2	Bidirectional	2.5 V	78
HSMC_TX_n5	G1	Bidirectional	2.5 V	79
HSMC_RX_n5	H1	Bidirectional	2.5 V	80
HSMC_TX_p6	K2	Bidirectional	2.5 V	83
HSMC_RX_p6	K5	Bidirectional	2.5 V	84
HSMC_TX_n6	K1	Bidirectional	2.5 V	85
HSMC_RX_n6	L5	Bidirectional	2.5 V	86
HSMC_TX_p7	L2	Bidirectional	2.5 V	89
HSMC_RX_p7	L4	Bidirectional	2.5 V	90
HSMC_TX_n7	L1	Bidirectional	2.5 V	91
HSMC_RX_n7	L3	Bidirectional	2.5 V	92
HSMC_TX_p8	M2	Bidirectional	2.5 V	101
HSMC_RX_p8	P2	Bidirectional	2.5 V	102
HSMC_TX_n8	M1	Bidirectional	2.5 V	103
HSMC_RX_n8	P1	Bidirectional	2.5 V	104
HSMC_TX_p9	R2	Bidirectional	2.5 V	107
HSMC_RX_p9	T3	Bidirectional	2.5 V	108
HSMC_TX_n9	R1	Bidirectional	2.5 V	109
HSMC_RX_n9	R3	Bidirectional	2.5 V	110
HSMC_TX_p10	E17	Bidirectional	2.5 V	113
HSMC_RX_p10	G17	Bidirectional	2.5 V	114
HSMC_TX_n10	E18	Bidirectional	2.5 V	115
HSMC_RX_n10	G18	Bidirectional	2.5 V	116
HSMC_TX_p11	H17	Bidirectional	2.5 V	119
HSMC_RX_p11	K18	Bidirectional	2.5 V	120
HSMC_TX_n11	H18	Bidirectional	2.5 V	121
HSMC_RX_n11	L18	Bidirectional	2.5 V	122

Table 2–9. HSMC Pinout (Part 3 of 3)

Signal Name	FPGA Pin Name	Direction	Type	HSMC Pin
HSMC_TX_p12	L17	Bidirectional	2.5 V	125
HSMC_RX_p12	L16	Bidirectional	2.5 V	126
HSMC_TX_n12	M18	Bidirectional	2.5 V	127
HSMC_RX_n12	M17	Bidirectional	2.5 V	128
HSMC_TX_p13	L14	Bidirectional	2.5 V	131
HSMC_RX_p13	L13	Bidirectional	2.5 V	132
HSMC_TX_n13	L15	Bidirectional	2.5 V	133
HSMC_RX_n13	M14	Bidirectional	2.5 V	134
HSMC_TX_p14	P17	Bidirectional	2.5 V	137
HSMC_RX_p14	R17	Bidirectional	2.5 V	138
HSMC_TX_n14	P18	Bidirectional	2.5 V	139
HSMC_RX_n14	R18	Bidirectional	2.5 V	140
HSMC_TX_p15	R5	Bidirectional	2.5 V	143
HSMC_RX_p15	M6	Bidirectional	2.5 V	144
HSMC_TX_n15	R4	Bidirectional	2.5 V	145
HSMC_RX_n15	N6	Bidirectional	2.5 V	146
HSMC_TX_p16	T17	Bidirectional	2.5 V	149
HSMC_RX_p16	M13	Bidirectional	2.5 V	150
HSMC_TX_n16	T18	Bidirectional	2.5 V	151
HSMC_RX_n16	N13	Bidirectional	2.5 V	152

Push Buttons

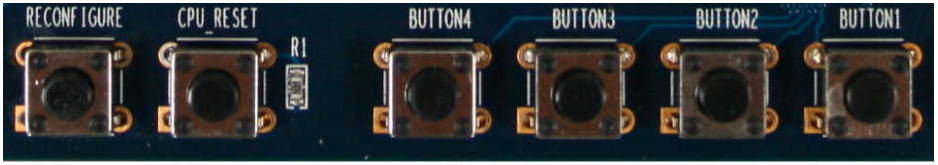
The board has system reset, user reset, and user push buttons. Table 2–10 lists the pinout for all push buttons. Push buttons are a logic "1" until depressed.

Table 2–10. Push Button Pinout

Signal Name	FPGA Pin	Direction	Type
KEY0	F1	Input	2.5 V
KEY1	F2	Input	2.5 V
KEY2	A10	Input	2.5 V
KEY3	B10	Input	2.5 V
CPU_RESET_N	N2	Input	2.5 V
RECONFIGURE	H5 (nConfig)	Input	2.5 V

Figure 2–5 shows the push buttons.

Figure 2–5. Push Buttons



System Reset Push Buttons

The system reset push button is used to force a re-configuration of the FPGA from flash memory.

User Reset Push Buttons

The user reset push button is an input to the Cyclone III device. It is intended to be the master reset signal for the FPGA designs loaded into the Cyclone III device. The user reset push button is connected to the `DEV_CLRn` pin on the FPGA. The `DEV_CLRn` setting is a pin option in the Quartus II software that you must enable to function as `DEV_CLRn` instead of a standard I/O.

User Push Buttons

The four user push buttons are intended for use in controlling FPGA designs loaded into the Cyclone III device. There is no board-specific function for these four push buttons.

LEDs

The board has user LEDs and board-specific LEDs. Table 2–11 lists both user and board-specific LED pinout. A logic "0" causes the LEDs to illuminate.

Table 2–11. Board LED Pinout (Part 1 of 2)

Signal Name	FPGA Pin Name	Direction	Type
LED0	P13	Output	2.5 V
LED1	P12	Output	2.5 V
LED2	N12	Output	2.5 V
LED3	N9	Output	2.5 V
Power LED	N/A	N/A	N/A

Table 2–11. Board LED Pinout (Part 2 of 2)			
Signal Name	**FPGA Pin Name**	**Direction**	**Type**
MAX Load LED	N/A	N/A	N/A
conf done LED	N/A	N/A	N/A
Flash LED	N/A	N/A	N/A
HSMC Present LED	N/A	N/A	N/A

Figure 2–6 shows the LEDs.

Figure 2–6. LEDs

User LEDs

Status and debugging signals are driven to the user LEDs from FPGA designs loaded into the Cyclone III device. There is no board-specific function for the user LEDs.

Board Specific LEDs

The power LED illuminates when the board's power is on and working. The configuration done LED illuminates when the FPGA is programmed.

- Configuration LED: The Conf_Done LED illuminates when the FPGA is successfully configured with any design
- Flash signal LED: The flash_CE_n LED illuminates when the CE_n signal to the flash is asserted indicating the flash is being accessed.
- Power LED: The power LED illuminates when power is applied to the board.

Memory

The Cyclone III FPGA starter board includes the following memories:

- Parallel flash
- DDR SDRAM
- SSRAM

Parallel Flash

The Cyclone III starter board has a 32M x 16 low voltage parallel flash. Table 2–12 lists the parallel flash board reference and manufacturing information.

Table 2–12. Parallel Flash Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number
U6	32M x16 low voltage parallel flash	Intel	PC28F256P30B85

Table 2–13 shows the parallel flash signal name, corresponding FPGA pin, signal direction, type and board reference U6 flash pin.

Table 2–13. Parallel Flash Memory Pinout (Part 1 of 2)

Signal Name	FPGA Pin	Direction	Type	U6 (Flash) Pin
flash_sram_a1	E12	Output	2.5 V	A1
flash_sram_a2	A16	Output	2.5 V	B1
flash_sram_a3	B16	Output	2.5 V	C1
flash_sram_a4	A15	Output	2.5 V	D1
flash_sram_a5	B15	Output	2.5 V	D2
flash_sram_a6	A14	Output	2.5 V	A2
flash_sram_a7	B14	Output	2.5 V	C2
flash_sram_a8	A13	Output	2.5 V	A3
flash_sram_a9	B13	Output	2.5 V	B3
flash_sram_a10	A12	Output	2.5 V	C3
flash_sram_a11	B12	Output	2.5 V	D3
flash_sram_a12	A11	Output	2.5 V	C4
flash_sram_a13	B11	Output	2.5 V	A5
flash_sram_a14	C10	Output	2.5 V	B5
flash_sram_a15	D10	Output	2.5 V	C5
flash_sram_a16	E10	Output	2.5 V	D7
flash_sram_a17	C9	Output	2.5 V	D8

Table 2–13. Parallel Flash Memory Pinout (Part 2 of 2)

Signal Name	FPGA Pin	Direction	Type	U6 (Flash) Pin
flash_sram_a18	D9	Output	2.5 V	A7
flash_sram_a19	A7	Output	2.5 V	B7
flash_sram_a20	A6	Output	2.5 V	C7
flash_sram_a21	B18	Output	2.5 V	C8
flash_sram_a22	C17	Output	2.5 V	A8
flash_sram_a23	C18	Output	2.5 V	G1
flash_sram_a24	G14	Output	2.5 V	H8
flash_sram_a25	B17	Output	2.5 V	B6
flash_sram_dq0	H3	Bidirectional	2.5 V	F2
flash_sram_dq1	D1	Bidirectional	2.5 V	E2
flash_sram_dq2	A8	Bidirectional	2.5 V	G3
flash_sram_dq3	B8	Bidirectional	2.5 V	E4
flash_sram_dq4	B7	Bidirectional	2.5 V	E5
flash_sram_dq5	C5	Bidirectional	2.5 V	G5
flash_sram_dq6	E8	Bidirectional	2.5 V	G6
flash_sram_dq7	A4	Bidirectional	2.5 V	H7
flash_sram_dq8	B4	Bidirectional	2.5 V	E1
flash_sram_dq9	E7	Bidirectional	2.5 V	E3
flash_sram_dq10	A3	Bidirectional	2.5 V	F3
flash_sram_dq11	B3	Bidirectional	2.5 V	F4
flash_sram_dq12	D5	Bidirectional	2.5 V	F5
flash_sram_dq13	B5	Bidirectional	2.5 V	H5
flash_sram_dq14	A5	Bidirectional	2.5 V	G7
flash_sram_dq15	B6	Bidirectional	2.5 V	E7
flash_we_n	D18	Output	2.5 V	G8
flash_ce_n	E2	Output	2.5 V	B4
flash_oe_n	D17	Output	2.5 V	F8
flash_reset_n	C3	Output	2.5 V	D4
flash_adv_n	H14	Output	2.5 V	F6
flash_clk (dclk)	H4	Output	2.5 V	E6
flash_wait	H13	Output	2.5 V	F7

DDR SDRAM

The Cyclone III FPGA starter board has a 4M x 16 x 4 DDR SDRAM. Table 2–14 lists DDR SDRAM board reference and manufacturing information.

Table 2–14. DDR SDRAM Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number
U4	4M x16 x 4 DDR SDRAM	PowerChip Semiconductor	A2S56D40CTP-G5PP

Table 2–15 shows the DDR SDRAM signal name, corresponding FPGA pin, signal direction, type and board reference U4 DDR pin.

Table 2–15. DDR SDRAM Pinout (Part 1 of 2)

Signal Name	FPGA Pin	Direction	Type	U4 (DDR) Pin
ddr_dqs0	U3	Bidirectional	SSTL-2	16
ddr_dqs1	T8	Bidirectional	SSTL-2	51
ddr_dm0	V3	Output	SSTL-2	47
ddr_dm1	V8	Output	SSTL-2	20
ddr_ba0	V11	Output	SSTL-2	26
ddr_ba1	V12	Output	SSTL-2	27
ddr_cas_n	T4	Output	SSTL-2	22
ddr_cke	R13	Output	SSTL-2	44
ddr_cs_n	V1	Output	SSTL-2	24
ddr_ras_n	V16	Output	SSTL-2	23
ddr_we_n	U15	Output	SSTL-2	21
ddr_clk	U2	Bidirectional	SSTL-2	45
ddr_clk_n	V2	Bidirectional	SSTL-2	46
ddr_a0	U1	Output	SSTL-2	29
ddr_a1	U5	Output	SSTL-2	30
ddr_a2	U7	Output	SSTL-2	31
ddr_a3	U8	Output	SSTL-2	32
ddr_a4	P8	Output	SSTL-2	35
ddr_a5	P7	Output	SSTL-2	36
ddr_a6	P6	Output	SSTL-2	37
ddr_a7	T14	Output	SSTL-2	38

Table 2–15. DDR SDRAM Pinout (Part 2 of 2)

Signal Name	FPGA Pin	Direction	Type	U4 (DDR) Pin
ddr_a8	T13	Output	SSTL-2	39
ddr_a9	V13	Output	SSTL-2	40
ddr_a10	U17	Output	SSTL-2	28
ddr_a11	V17	Output	SSTL-2	41
ddr_a12	U16	Output	SSTL-2	42
ddr_dq0	U4	Bidirectional	SSTL-2	2
ddr_dq1	V4	Bidirectional	SSTL-2	4
ddr_dq2	R8	Bidirectional	SSTL-2	5
ddr_dq3	V5	Bidirectional	SSTL-2	7
ddr_dq4	P9	Bidirectional	SSTL-2	8
ddr_dq5	U6	Bidirectional	SSTL-2	10
ddr_dq6	V6	Bidirectional	SSTL-2	11
ddr_dq7	V7	Bidirectional	SSTL-2	13
ddr_dq8	U13	Bidirectional	SSTL-2	54
ddr_dq9	U12	Bidirectional	SSTL-2	56
ddr_dq10	U11	Bidirectional	SSTL-2	57
ddr_dq11	V15	Bidirectional	SSTL-2	59
ddr_dq12	U14	Bidirectional	SSTL-2	60
ddr_dq13	R11	Bidirectional	SSTL-2	62
ddr_dq14	P10	Bidirectional	SSTL-2	63
ddr_dq15	V14	Bidirectional	SSTL-2	65

SSRAM

The Cyclone III FPGA starter board has a 256K x 32 synchronous SRAM. Table 2–16 lists SSRAM board reference and manufacturing information.

Table 2–16. SSRAM Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number
U5	256K x 32 synchronous SRAM	Integrated Silicon Solutions, Inc.	IS61LPS25636A-200TQL1

Table 2–17 shows the SSRAM signal name, corresponding FPGA pin, signal direction, type and board reference U5 SSRAM pin.

Table 2–17. SSRAM Pinout (Part 1 of 2)

Signal Name	FPGA Pin	Direction	Type	U5 (SSRAM) Pin
flash_sram_a2	A16	Output	2.5 V	37
flash_sram_a3	B16	Output	2.5 V	36
flash_sram_a4	A15	Output	2.5 V	35
flash_sram_a5	B15	Output	2.5 V	34
flash_sram_a6	A14	Output	2.5 V	33
flash_sram_a7	B14	Output	2.5 V	32
flash_sram_a8	A13	Output	2.5 V	44
flash_sram_a9	B13	Output	2.5 V	45
flash_sram_a10	A12	Output	2.5 V	46
flash_sram_a11	B12	Output	2.5 V	47
flash_sram_a12	A11	Output	2.5 V	48
flash_sram_a13	B11	Output	2.5 V	49
flash_sram_a14	C10	Output	2.5 V	50
flash_sram_a15	D10	Output	2.5 V	81
flash_sram_a16	E10	Output	2.5 V	82
flash_sram_a17	C9	Output	2.5 V	99
flash_sram_a18	D9	Output	2.5 V	100
flash_sram_a19	A7	Output	2.5 V	43
flash_sram_a20	A6	Output	2.5 V	42
flash_sram_a21	B18	Output	2.5 V	39
flash_sram_a22	C17	Output	2.5 V	38
flash_sram_dq0	H3	Bidirectional	2.5 V	52
flash_sram_dq1	D1	Bidirectional	2.5 V	53
flash_sram_dq2	A8	Bidirectional	2.5 V	56
flash_sram_dq3	B8	Bidirectional	2.5 V	57
flash_sram_dq4	B7	Bidirectional	2.5 V	58
flash_sram_dq5	C5	Bidirectional	2.5 V	59
flash_sram_dq6	E8	Bidirectional	2.5 V	62
flash_sram_dq7	A4	Bidirectional	2.5 V	63
flash_sram_dq8	B4	Bidirectional	2.5 V	68
flash_sram_dq9	E7	Bidirectional	2.5 V	69
flash_sram_dq10	A3	Bidirectional	2.5 V	72

Table 2–17. SSRAM Pinout (Part 2 of 2)

Signal Name	FPGA Pin	Direction	Type	U5 (SSRAM) Pin
flash_sram_dq11	B3	Bidirectional	2.5 V	73
flash_sram_dq12	D5	Bidirectional	2.5 V	74
flash_sram_dq13	B5	Bidirectional	2.5 V	75
flash_sram_dq14	A5	Bidirectional	2.5 V	78
flash_sram_dq15	B6	Bidirectional	2.5 V	79
flash_sram_dq16	C16	Bidirectional	2.5 V	2
flash_sram_dq17	D12	Bidirectional	2.5 V	3
flash_sram_dq18	E11	Bidirectional	2.5 V	6
flash_sram_dq19	D2	Bidirectional	2.5 V	7
flash_sram_dq20	E13	Bidirectional	2.5 V	8
flash_sram_dq21	E14	Bidirectional	2.5 V	9
flash_sram_dq22	A17	Bidirectional	2.5 V	12
flash_sram_dq23	D16	Bidirectional	2.5 V	13
flash_sram_dq24	C12	Bidirectional	2.5 V	18
flash_sram_dq25	A18	Bidirectional	2.5 V	19
flash_sram_dq26	F8	Bidirectional	2.5 V	22
flash_sram_dq27	D7	Bidirectional	2.5 V	23
flash_sram_dq28	F6	Bidirectional	2.5 V	24
flash_sram_dq29	E6	Bidirectional	2.5 V	25
flash_sram_dq30	G6	Bidirectional	2.5 V	28
flash_sram_dq31	C7	Bidirectional	2.5 V	29
sram_oe_n	E9	Output	2.5 V	86
sram_ce1_n	F9	Output	2.5 V	98
sram_we_n	G13	Output	2.5 V	87
sram_be_n0	F10	Output	2.5 V	93
sram_be_n1	F11	Output	2.5 V	94
sram_be_n2	F12	Output	2.5 V	95
sram_be_n3	F13	Output	2.5 V	96
sram_adsc_n	F7	Output	2.5 V	85
sram_clk	A2	Output	2.5 V	89

Power Supply

The power supply block distributes clean power from the 12 V input supply to the Cyclone III device through on-board regulators.

To provide various voltage options, the board uses several Linear Technologies' regulators. Switching regulators are used for digital circuits and linear regulators are used for analog circuits. Board regulators are used to generate the voltages listed in Table 2–18.

Table 2–18. Board Regulators

Output Voltage (V)	Variance (+/- mV)	MAX Current (A)	Board Access Point	Regulator Board Reference	Linear Technologies Part #	Where Used
1.20	50	3.0	JP6 *(1)*	REG4	LT1959CS8	Cyclone III Core voltage
1.25	50	1.0	JP4	REG2	LTC3413	DDR termination voltage
2.50	50	6.0	JP3 *(1)*	REG1	LTM4603EV	DDR, SRAM, Flash, PLLs, other bias voltages
1.80	80	1.5	JP7	REG5	LT1959CS8	Parallel flash interface, USB buffers and other I/O
3.30	100	2.0	JP5	REG3	LT1959CS8	I/O voltage and power for most components including HSMC
12.00	200	1.0	SW1	N/A	N/A	Input supply voltage. All other voltages (including HSMC voltage) are derive from this regulator.

Note to Table 2–18:
(1) A 0.01 current sense resistor has been added to select jumper points for FPGA core power and I/O power measurement.

You can measure the core and I/O voltage with a current meter while the Cyclone III device is in standby mode. For more information on this circuit, refer to the *Cyclone III FPGA Starter Kit Getting Started User Guide*.

Statement of China-RoHS Compliance

Table 2–19 lists hazardous substances included with the kit.

Table 2–19. Table of Hazardous Substances' Name and Concentration, Notes (1),(2)

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavalent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Cyclone III FPGA starter board	X*	0	0	0	0	0
12 V power supply	0	0	0	0	0	0
Type A-B USB cable	0	0	0	0	0	0
User guide	0	0	0	0	0	0

Notes to Table 2–19:

(1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

(2) X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.