HSTC Adaptor Card



This document illustrates the function and relative factors of each connector adaptor card which is used for HSTC connector. HSTC connector is a 180pin high speed connector designed by Terasic. The connector is fully compatible with Altera HSMC connector as well. Terasic provides a series of HSTC connector adaptor card which gives users more flexibility when utilizing the interfaces of HSTC connector. In addition to this, we also provide a testing adaptor card which enables the users to perform a self-test over the I/O pins on the HSTC connector. Several models of HSTC connector adaptor cards are ready for you now:

- THDB_HFF
- THDB_HMM
- THDB_HTR
- THDB_HLB
- THDB_SFF
- THDB_CFF

The chapters below demonstrate the detailed function and usage.

1. THDB_HFF

As shown in Figure 1 and Figure 2, THDB_HFF adaptor card has Female Pin Heads on both sides of the bard. To connect two HSTC connectors, which are both Mail Pin Heads, users can easily achieve the connection with the THDB_HFF adaptor card. Figure 3 illustrates how to connect TRDB_H2G(male HSTC connector) with a DE3 board (male HSTC connector).



Figure 1. The top view of the THDB_HFF





Figure 3. The connection setup for DE3 board and TRDB_H2G via THDB_HFF

2. THDB_HMM

THDB_HMM adaptor card, on the other hand, has two Male Pin Heads on the both sides per se as shown in Figure 4 and Figure 5. Users can connect two Female HSTC connector card with THDB_HMM adaptor card.



Figure 5. The bottom view of the THDB_HMM

3. THDB_HTR

THDB_HTR adaptor card provides a Male and a Female Pin Head of HSTC connector. The I/O pins of the both sides (i.e., the male side and the female side) are inter connected. By this delicate design (see Figure 6), users can conduct the TX signal and the RX signal coming from

both upper side and lower side in the differential pattern via THDB_HTR adaptor card. Figure 7 and Figure 8 are the both sides of the THDB_HMM adaptor card.



Figure 6. The signal flow for THDB_HTR adaptor card



Figure 8. The bottom view of the THDB_HTR

4. THDB_HLB

THDB_HLB is designed to test the functionality of the I/O pins on the HSTC connector. As shown in Figure 9, the I/O pins on the left and the I/O pins on the right are connected as short. Users can install the THDB_HLB onto the HSTC connector for testing. By sending signals to one end and receiving signals from the other end, users can see if all the I/O pins are functional. Figure 10 and Figure 11 illustrates the both sides of the THDB_HLB.

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HSTC_CLKIN_n1		1	2 4	HSTC_CLKIN_n1	
HSTC_CLKIN_p1	5	3 -	4 6	HSTC_CLKIN_p1	
UOTO DY 10	7.	2 8	8		
HSTC_RX_NU	9	9	10 12	HSTC_RX_n0	
пото_кл_ро	11	-11	12 14	Пате_кх_ро	
HSTC_RX_n1	15	-13	14 16	HSTC RX n1	
HSTC_RX_p1	17 📕	15	16 18	HSTC_RX_p1	
	18	17	18 <u>20</u>		
HSTC_RX_n2	21	21 8	22 22	HSTC_RX_n2	
НЪТС_КХ_Р2	23	23	24 26	HSTC_RX_p2	
HSTC RX n3	25	25	26 28	HSTC RX n3	
HSTC_RX_p3	39	27	28 30	HSTC_RX_p3	
	31	39	30 32		
HSTC_RX_n4	33	33	34 34	HSTC_RX_n4	
HSIC_RX_p4	35	35	36 36	HSIC_RX_p4	
HSTC RX n5	37	37 m	38 40	HSTC BX n5	
HSTC_RX_p5	41	39 🖉	40 42	HSTC_RX_p5	
	43	41	42 44		
HSTC_RX_n6	45	43	44 46	HSTC_RX_n6	
HSTC_RX_p6	47	47	48 48	HSTC_RX_p6	
HSTC RX n7	49	49	50 52	HSTC RX n7	
HSTC RX p7	51	51	52 54	HSTC_RX_I7	
	55	53 4	54 56	Here_inc_pr	
HSTC_RX_n8	57	55 2	56 58	HSTC_RX_n8	
		- 3/	⁵⁰ 60	HSTC RX p8	
HSTC_RX_p8	59,	59	60		
HSTC_RX_p8	59	59	60		
HSTC_RX_p8	59	-59 -61	60 62 62 64	HSTC CLKIN #2	
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HSTC_RX_p8	59 61 63 65 66 67	59 61 63 63 82	60 62 62 64 64 66 66 66 68	HSTC_CLKIN_n2 HSTC_CLKIN_p2	
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Figure 9. The schematic of the THDB_HLB



Figure 10. The top view of the THDB_HLB



Figure 11. The bottom view of the THDB_HLB

5. THDB_SFF

THDB_SFF adapter card is designed for bypassing JTAG signal form host board to daughter board via a one-position dip switch (Please refer to Figure 12 and Figure 13). When HSTC daughter board connects HOST board through THDB_SFF, HSTC daughter board can bypass the signal of JTAG interface from TDO to TDI. Figure 14 and Figure 15 are the both sides of the THDB_HMM adaptor card.



Figure 12. The signal flow for THDB_SFF adaptor card



Figure 13. The one-position dip switch for JTAG interface control



Figure 14. The top view of the THDB_SFF



Figure 15. The bottom view of the THDB_SFF

6. THDB_CFF

THDB_CFF can switch the clock pair, HSTC_CLKIN_0 and HSTC_CLKIN_1, between two HSTC interface boards. In other words, the "clock pair HSTC_CLKIN_0" of HSTC interface board A pass through THDB_CFF adaptor card and then connect with the clock pair HSTC_CLKIN_1 of HSTC interface board B (See Figure 16).

In addition, THDB_CFF has the same function as THDB_SFF adaptor card, it can bypass the JTGA interface signal via a one-position dip switch.Figure 17 and Figure 18 are the both sides of the THDB_HMM adaptor card.



Figure 16. The signal flow for THDB_CFF adaptor card



Figure 17. The top view of the THDB_CFF



Figure 18. The bottom view of the THDB_CFF

Revision History

Date	Version	Changes
2008.6	First publication	
2008.11	v.1.1	1. Add descriptions for THDB-SFF and THDB-CFF