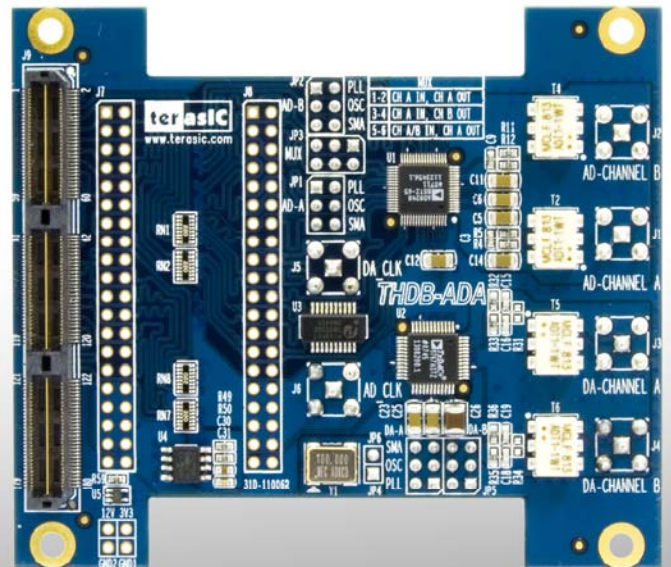
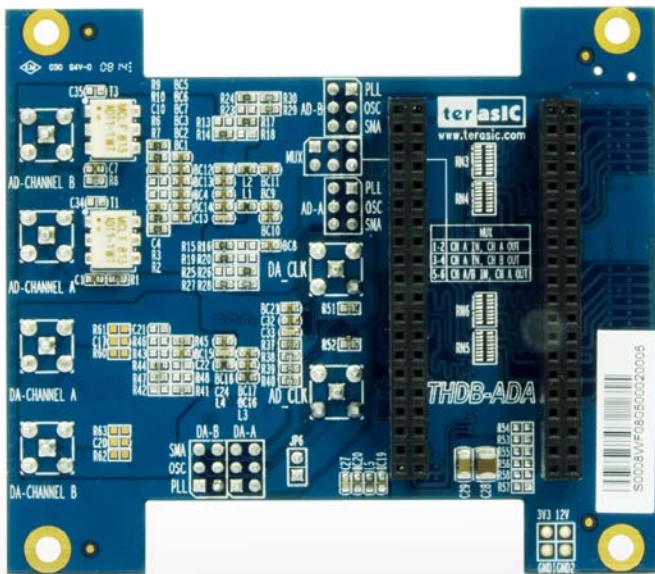


THDB_ADA

High-Speed A/D and D/A Development Kit

With complete reference design and source code for Fast-Fourier Transform analysis and arbitrary waveform generator.



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About the Kit

The THDB_ADA (ADA) daughter board is designed to provide DSP solution on DE series and Cyclone III Starter Kit, or other boards with HSMC or GPIO interface. It is equipped with one ADC (Analog-to-Digital Converter) and DAC (Digital-to-Analog Converter) each, to provide dual-channel ports. This chapter provides users key information about the kit.

1-1 Kit Contents

Figure 1.1 and Figure 1.2 show the picture of the ADA-HSMC and ADA-GPIO package, respectively. The package includes:

1. The Terasic **Analog-to-Digital** and **Digital-to-Analog (ADA)** board
2. Complete reference design with source code

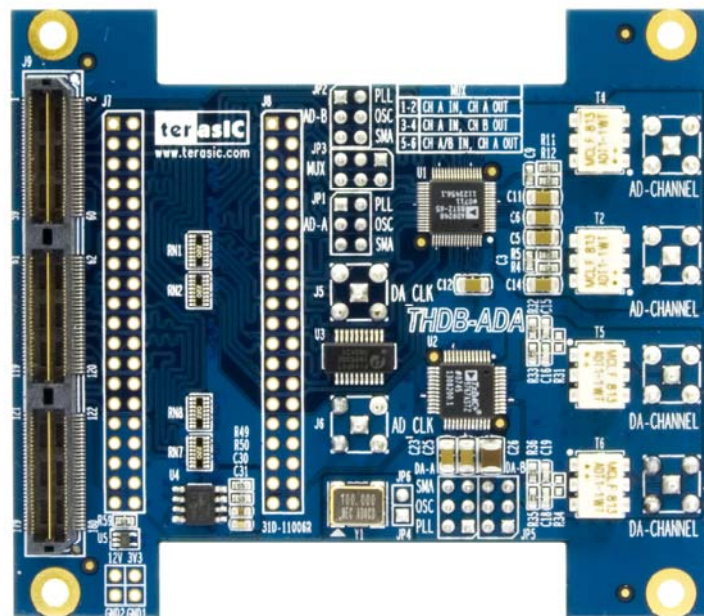


Figure 1.1 ADA-HSMC

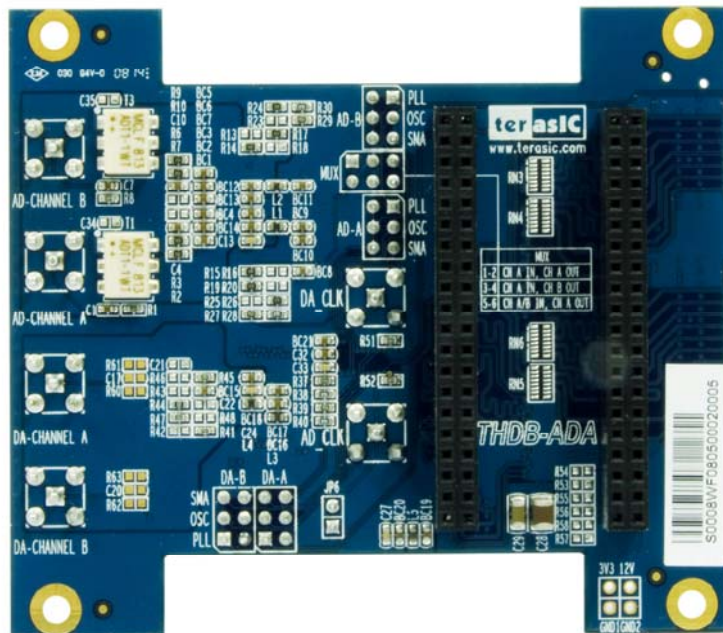


Figure 1.2 ADA-GPIO

1-2 Connectivity

There are two models available, ADA-GPIO and ADA-HSMC, which offer the compatibility of connecting the THDB_ADA (ADA) kit to DE2-70/DE2/DE1 and DE3/Cyclone III Starter Kit, respectively.

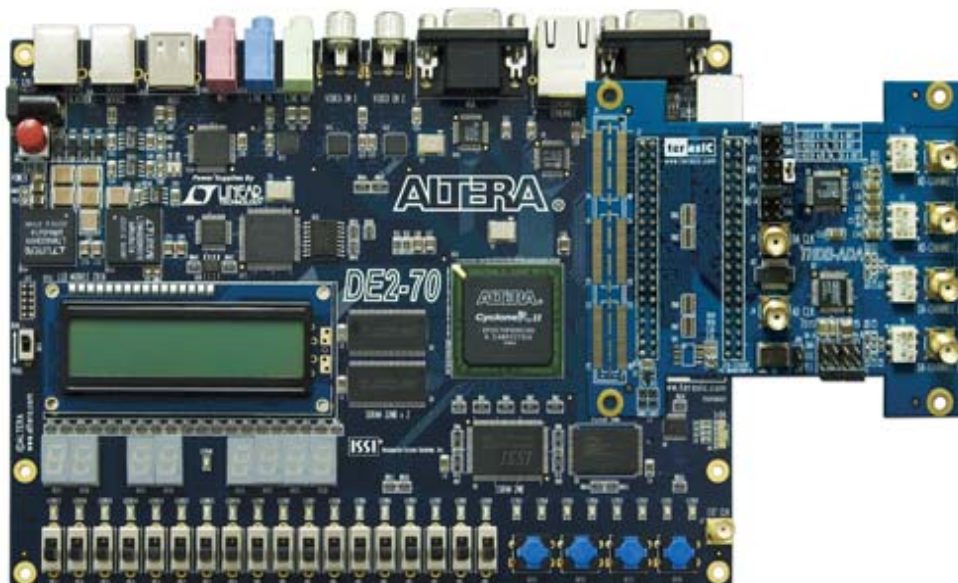


Figure 1.3 Connect ADA-GPIO with DE2-70

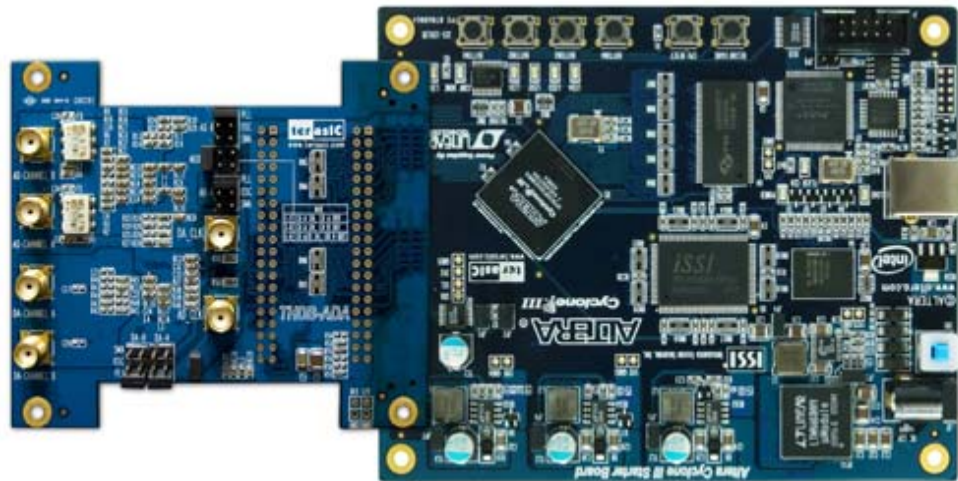


Figure 1.4 Connect ADA-HSMC with Cyclone III Starter Kit

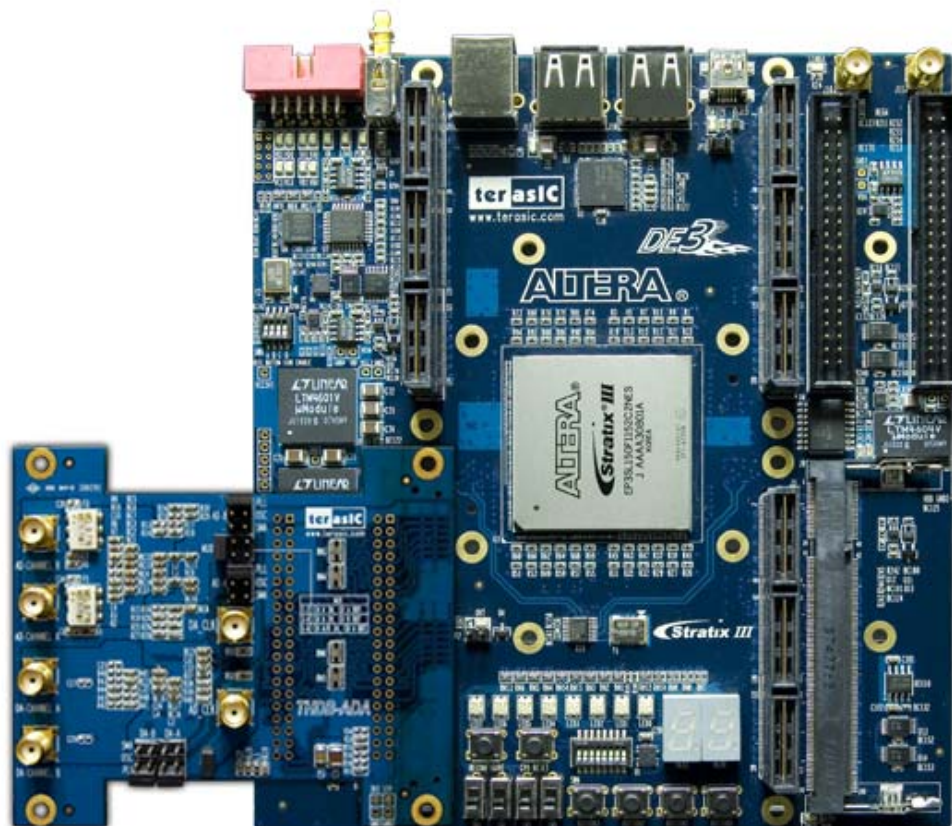


Figure 1.5 Connect ADA- HSMC with DE3

1-3 Getting Help

Here are some places to get help if you encounter any problem:

- ✓ Email to support@terasic.com
- ✓ Taiwan & China: +886-3-550-8800
- ✓ Korea : +82-2-512-7661
- ✓ Japan: +81-428-77-7000

Architecture of the ADA

This chapter will illustrate the architecture of the ADA including device features and applications.

2-1 Features

The feature set of the ADA is listed below:

1. Dual AD channels with 14-bit resolution and data rate up to 65 MSPS
2. Dual DA channels with 14-bit resolution and data rate up to 125 MSPS
3. Dual interfaces include HSMC and GPIO, which are fully compatible with Cyclone III Starter Kit and DE1/DE2/DE3, respectively
4. Clock sources include oscillator 100MHz, SMA for AD and DA each, and PLL from either HSMC or GPIO interface

2-2 Applications

The feature set of the ADA is listed below:

1. Dual AD channels with 14-bit resolution and data rate up to 65 MSPS
2. Dual DA channels with 14-bit resolution and data rate up to 125 MSPS
3. Dual interfaces include HSMC and GPIO, which are fully compatible with Cyclone III Starter Kit and DE1/DE2/DE3, respectively
4. Clock sources include oscillator 100MHz, SMA for AD and DA each, and PLL from either HSMC or GPIO interface

Using the ADA

This chapter illustrates some special features of the ADA including interleaved data mode for digital-to-analog converter and multiplexed data mode for analog-to-digital converter.

3-1 Digital-to-Analog Converter

This section will describe the interleaved data mode for D/A converter of the ADA.

The DAC integrates two 14-bit TxDAC+ cores with dual-port input, while supporting refresh rate up to 125 MSPS. The dual-channel makes it capable of transmitting different data to two separate ports with different update rates. But it is the interleaving mode that makes it special, especially for processing I and Q data in communication applications. The input data stream is demuxed into its original I and Q data and latched. In the next phase they are converted by the two TxDAC+ cores and updated at half the input data rate. Figure 3.1 shows the timing of DAC in interleaved mode.

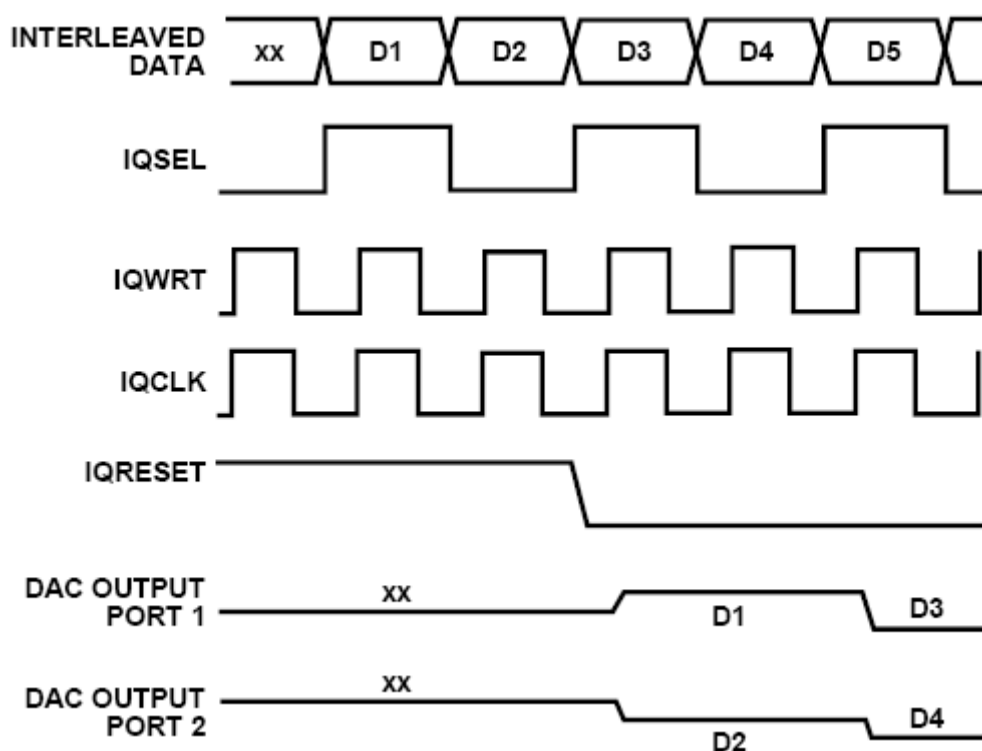


Figure 3.1 Interleaved Mode Timing

3-2 Analog-to-Digital Converter

This section will describe the multiplexed data mode for A/D converter of the ADA.

The ADC features dual sample-and-hold amplifiers with data rate up to 65 MSPS at the resolution of 14-bit. Its dual-channel inputs can also operate as two independent ports with different clock rates. Based on the state of the MUX option, multiplexed data output can be achieved by mixing data from the dual ports and the data rate is twice the sample rate. Figure 3.2 shows the multiplexed data format using the channel A output and the same clock tied to clock inputs of port A and B, and the selection of MUX option.

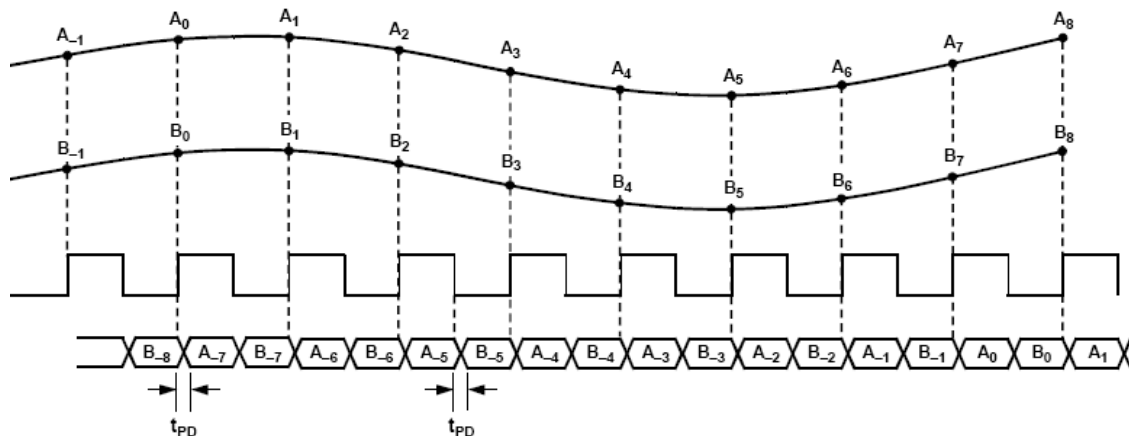


Figure 3.2 Multiplexed Data Format using the Channel A Output

ADA Demonstration

This chapter illustrates how to setup the ADA kit as an arbitrary waveform generator and evaluate the performance of A/D and D/A converter.

4-1 Arbitrary Waveform Generator

This section illustrates the implementation of random waveform generator using ADA. Figure 4.1 is the complete setup of an ADA connected on DE3. Simply perform the following steps to display any pattern generated from PC-based GUI on an oscilloscope. The *<path>* is the directory where you copy the reference design folder, DE3_ADA, from CD to your PC.

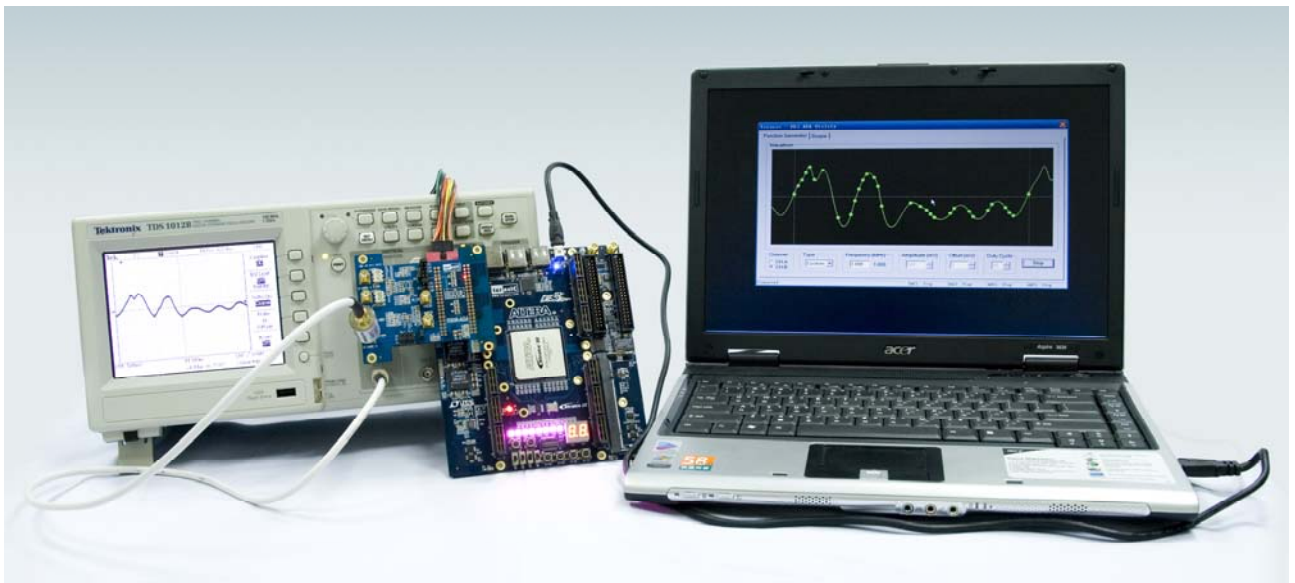


Figure 4.1 Configuration Setup of Random Waveform Generator on DE3

Configuring the Board:

1. Connect the ADA-HSMC to DE3, as shown in Figure 5.
2. Use a SMA cable to connect DA-Channel B with an oscilloscope..
3. For DAC B clock, add a jumper to JP5 with pins labeled PLL.
4. Use a USB cable to connect DE3 with PC
5. Power-on DE3
6. Open **DE3_ADA.qsf** from *<path>*\Demonstrations\DE3_ADA

7. Open *Quartus Programmer* from Tools -> Programmer
8. Press *Start* on the left-hand side.

Starting PC-Based Graphical User Interface:

1. Open *ADA_Utility.exe* from $\langle path \rangle \backslash ADA_Utility$
2. Use your mouse to draw a custom waveform from left to right. You may drag it or add more points to be sampled later on.
3. Set the frequency and the amplitude.
4. Press *Start*
5. Press *Autoset* on the oscilloscope if necessary.

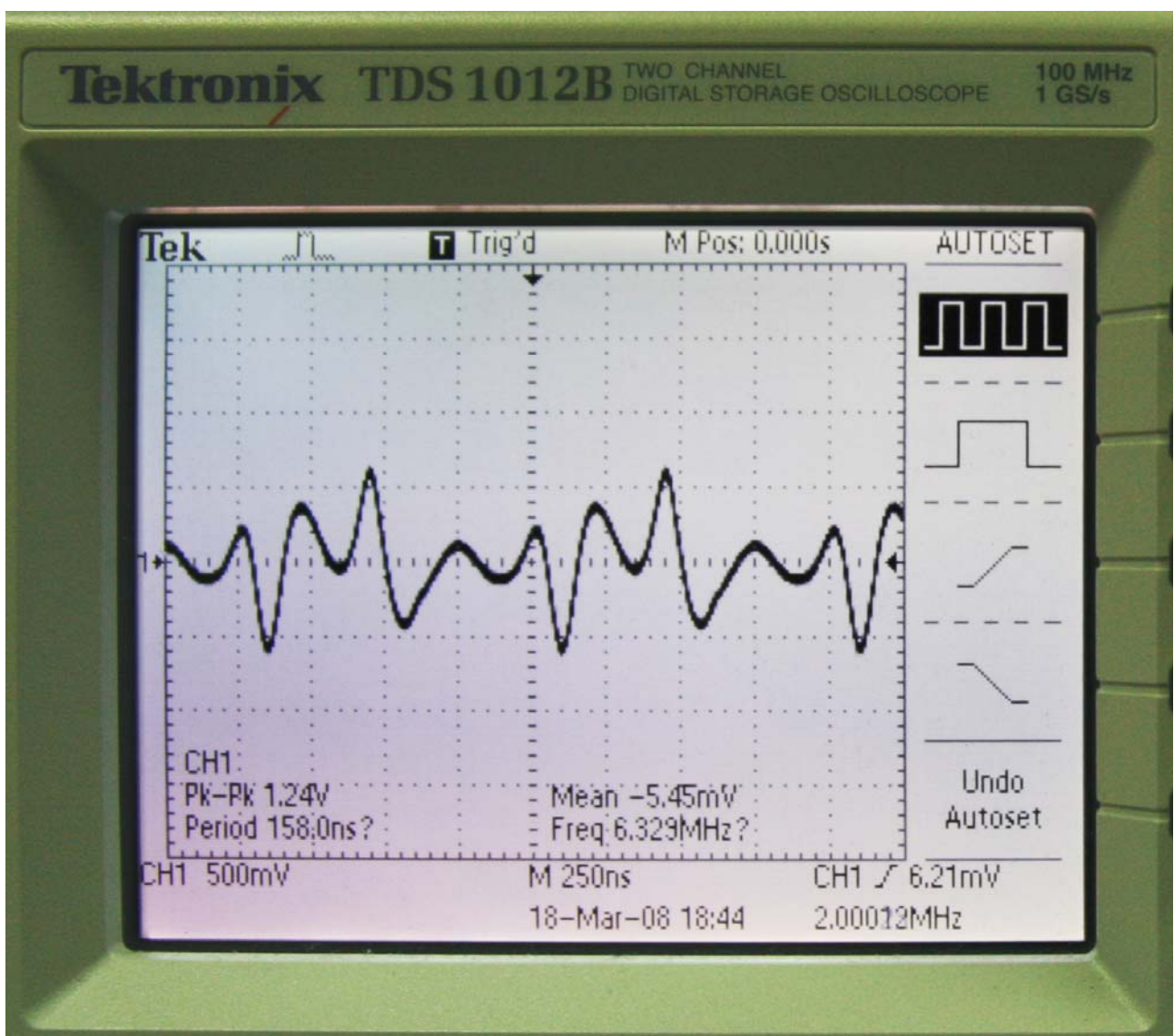


Figure 4.2 Pattern generated from DAC Channel-B is displayed on an oscilloscope.

4-2 A/D and D/A Converter Performance Evaluation

This section illustrates the steps to evaluate the performance of A/D and D/A converter on ADA, based on the data collected from DE2-70. Similar steps can also be applied to DE2/DE1 or Cyclone III Starter Kit. The `<path>` is the directory where you copy the reference design folder, DE2_70_ADA, from CD to your PC.

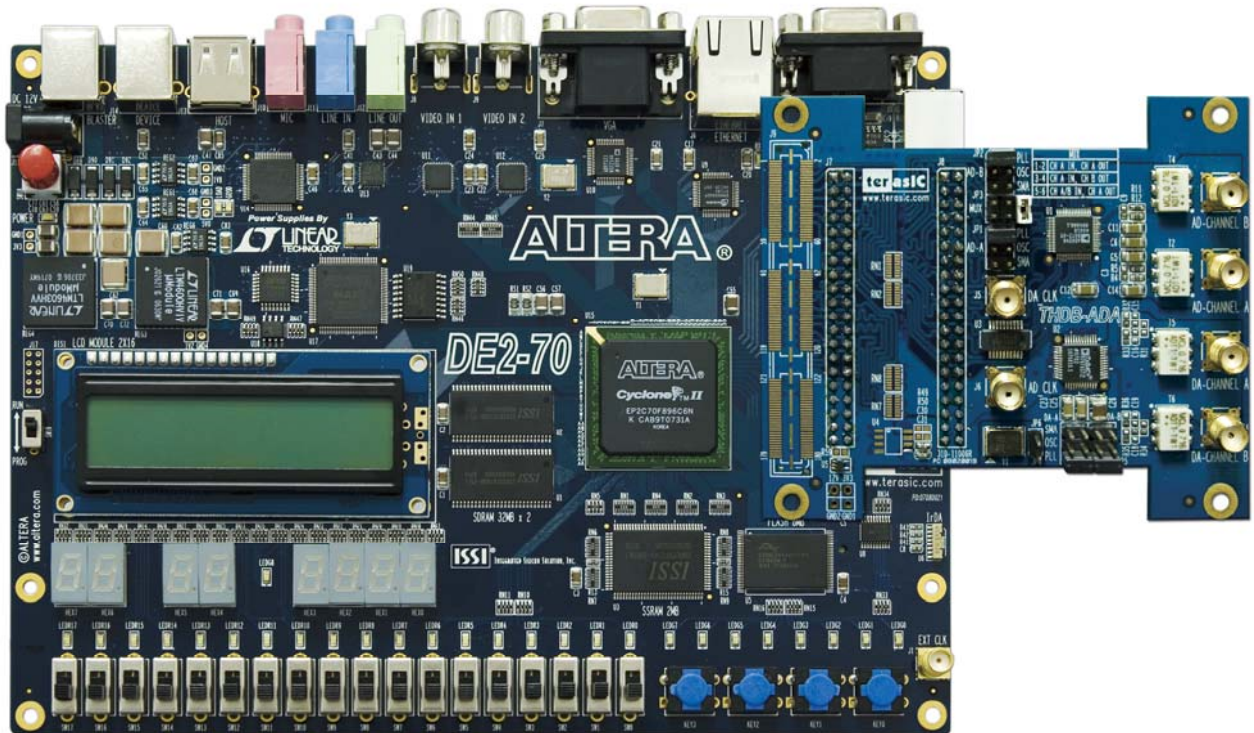


Figure 4.3 Connect ADA-GPIO with DE2-70

Configuring the Board:

1. Connect the ADA-GPIO to DE2-70, as shown in Figure 4.3.
2. Use a SMA cable to connect DA-Channel B with AD-Channel B.
3. Use a USB cable to connect DE2-70 with PC
4. Add appropriate jumpers for the mode and the clocks.
 - a. For DAC B clock, add a jumper to JP5 with pins labeled PLL.
 - b. For ADC B clock, add a jumper to JP2 with pins labeled PLL.
 - c. For the selection of MUX option, add a jumper to JP3, between pins 1 and 2.
5. Power-on DE2-70
6. Open **stp1.stp** from `<path>\Demonstrations\DE2_70_ADA`, as shown in Figure 4.4.

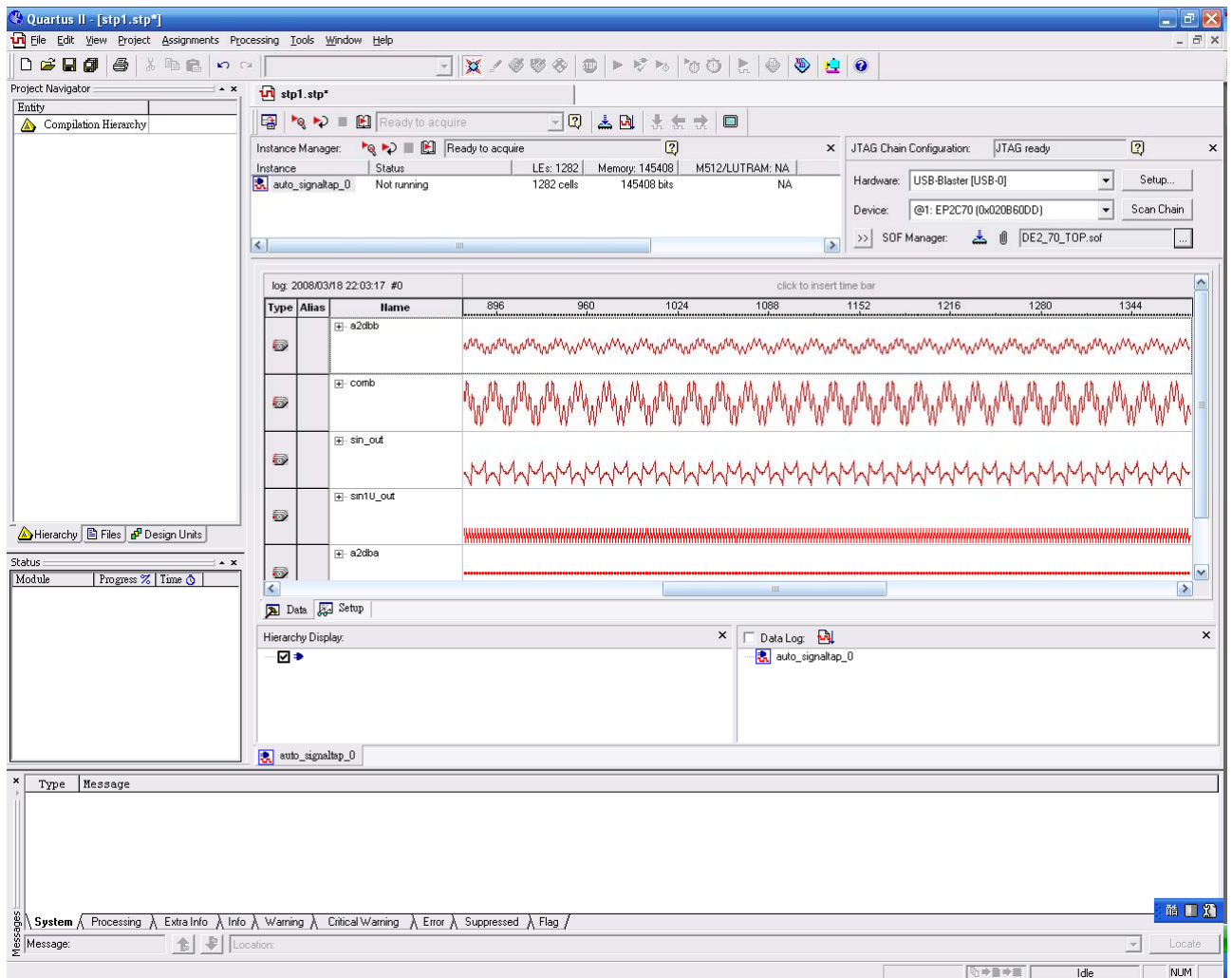


Figure 4.4 Connect ADA-GPIO with DE2-70

Collecting Data Using the SignalTap II Logic Analyzer

1. Click “Program Device” after Hardware and Device are detected correctly.
2. Click “Run Analysis” and observe signals *a2dbb* and *comb*, which shows attenuated and original combinations of two sine waves, respectively.
3. Choose File -> Create/Update -> Create SignalTap II List File and the Quartus II will generate the file `stp1_auto_sigtap_0.txt` in the project directory.

Analyzing the Data in the MATLAB Software

1. Start the MATLAB software.
2. Make sure the current directory is set to `<path>\Demonstrations\DE2_70_ADA`
3. Copy the file `nstp_plot.m` from `<path>\MATLAB` to `<path>\Demonstrations\DE2_70_ADA`

4. Type `nstf_plot('stp1_auto_sigaltap_0.txt')` at the MATLAB command prompt. The MATLAB will display normalized FFT plots of DAC B input and ADC B output similar to Figure 10 and Figure 11, respectively.

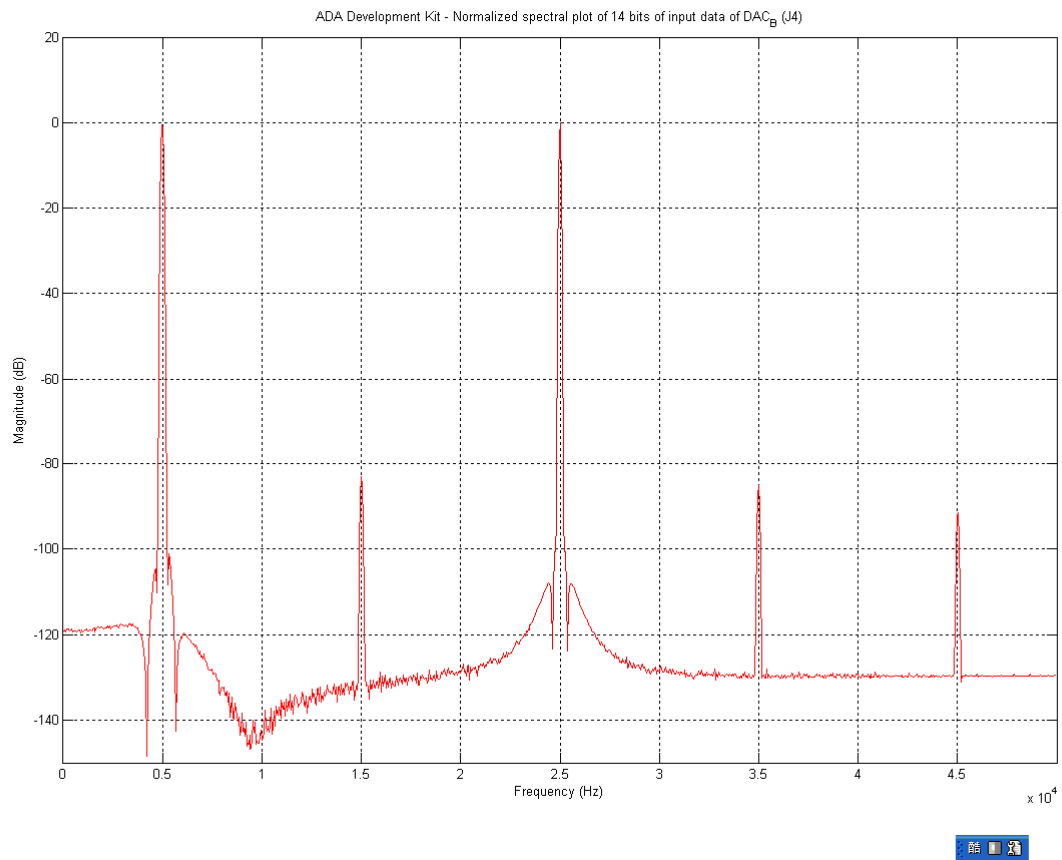


Figure 4.5 Normalized Spectral Plot of The 14-bit DAC B Input Data

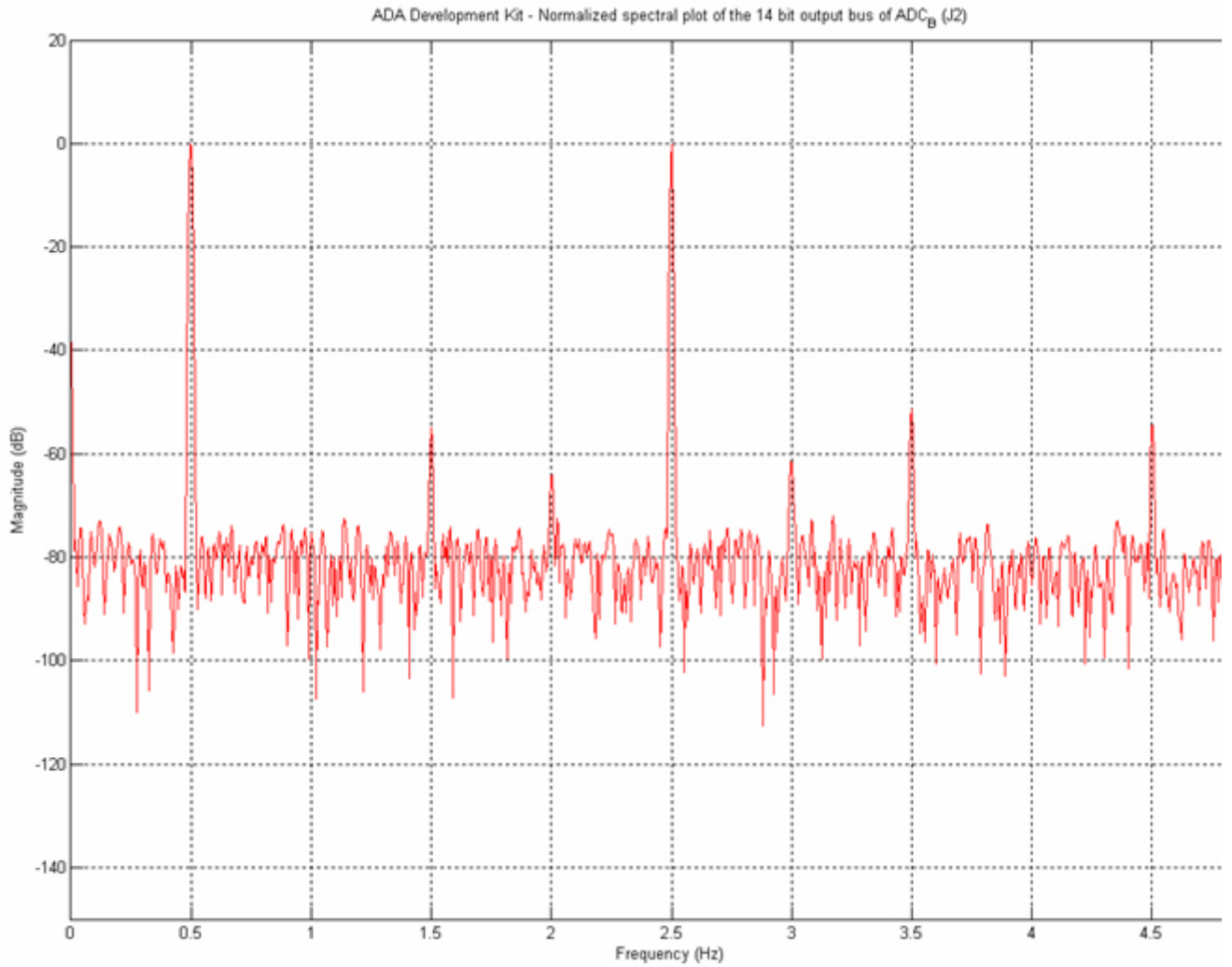


Figure 4.6 Normalized Spectral Plot of The 14-bit ADC B Output Data

5-1 Revision History

Version	Change Log
V1.0	Initial Version (Preliminary)
V1.1	Add Default Demo for DE1 and DE2

5-2 Always Visit Terasic Webpage for New Applications

We will continually provide interesting examples and labs on our ADA webpage.

Please visit www.terasic.com for more information.