Microbolometer Setup Instructions

1. FPGA cable assignments are located with the cables.
2. The microbolometer is a Photon 320.
3. The VHDL project to use is 320_ethernet
4. The FPGA board to use is the ML-506.
5. The bitstream file to use is already present in the 320_ethernet directory. The VHDL does not need to be recompiled; the FPGA merely needs to be programmed. Programming instructions are included with the project documentation.
6. The Ethernet driver does not work.
7. A Camera Link cable is used to connect the FPGA to the computer framegrabber. A breakout cable is located between the FPGA and the Camera Link cable.
8. The Camera Link output is 324 columns x 256 rows x 14 bits, monochrome.
9. For the Matlab display and acquisition software in the project, use Matlab R2010b SP2, 32 bit version.
10. The camera is connected to the cable labeled "Photon 320 camera". The serial port on the camera cable is NOT to be connected to the serial port on the FPGA board.
11. The configuration dip switches on the FPGA board must be set for the 320. These settings are in the project documentation.
12. The FPGA is connected to the Camera Link cable using the cable labeled "Photon 320 Camera Link"

FPGA Wiring Instructions

1. Connector headers go in the differential column of J4 on the ML-506 board.
2. The header from the Photon 320 breakout cable is plugged in such that the wires are connected to the differential column of J4, with the port marked "22" connected to pin 2 and the other ports connected in increasing order.

Camera Link Breakout Cable

The connector headers on the Camera Link breakout cable are connected to the differential column of J4, as shown in the chart below.

Twisted Pair Colors	Wire 1/Pin 1	Wire 2/Pin 2	Notes
Red, White	White/18	Red/20	Arrow at position 20
Green, Red	Red/22	Green/24	Arrow at position 24
Yellow, Brown	Brown/26	Yellow/28	Arrow at position 28
Pink, Black	Black/30	Pink/32	Arrow at position 32
Brown, White	White/34	Brown/36	Arrow at position 36

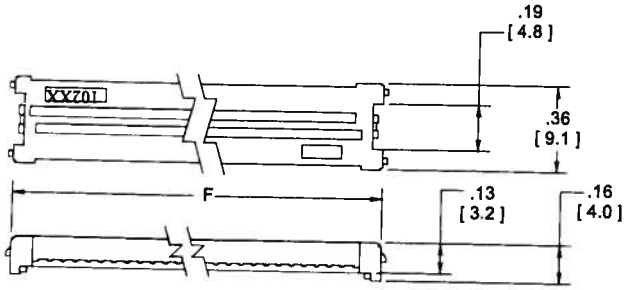
To use the chart, chose a wire pair listed in column 1. Plug in the connector such that the arrow is at the position located in column 4. The individual wires should thereby be connected as shown in columns 2 and 3.

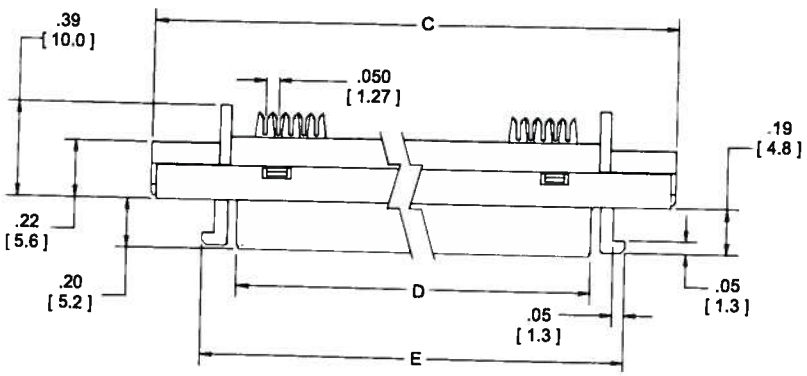
3M™ Mini D Ribbon (MDR) Connectors

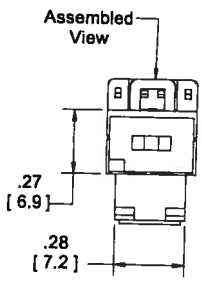
.050" IDC Wiremount Panelmount Receptacle - Shielded

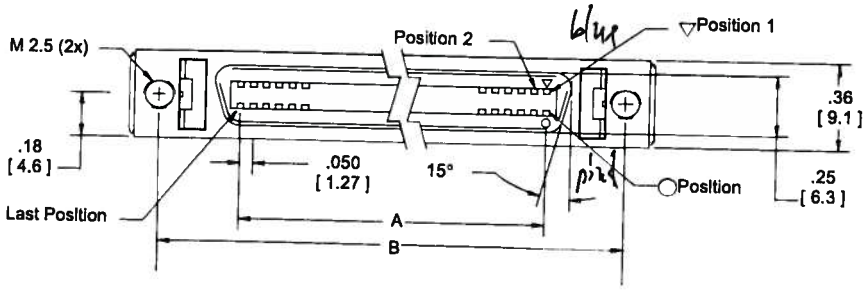
102 Series

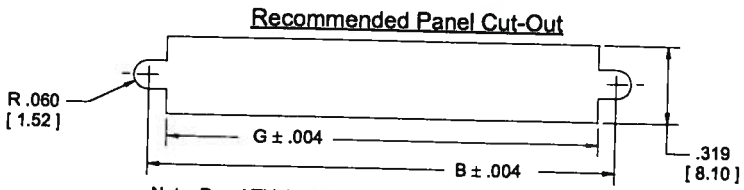
Contact Quantity	Dimensions						
	A	B	C	D	E	F	G
20	.450 [11.43]	1.081 [27.45]	1.31 [33.4]	.65 [16.4]	.92 [23.4]	.71 [18.0]	.94 [23.8]
26	.600 [15.24]	1.231 [31.26]	1.46 [37.2]	.80 [20.2]	1.07 [27.2]	.86 [21.8]	1.09 [27.6]
36	.850 [21.59]	1.481 [37.61]	1.71 [43.5]	1.05 [26.6]	1.32 [33.5]	1.11 [28.1]	1.33 [33.9]
40	.950 [24.13]	1.581 [40.15]	1.81 [46.1]	1.15 [29.1]	1.42 [36.1]	1.21 [30.7]	1.44 [36.5]
50	1.200 [30.48]	1.831 [46.50]	2.06 [52.4]	1.40 [35.5]	1.67 [42.4]	1.46 [37.0]	1.69 [42.8]
68	1.650 [41.91]	2.281 [57.93]	2.51 [63.8]	1.85 [46.9]	2.12 [53.8]	1.91 [48.4]	2.13 [54.2]











Note: Panel Thickness .079 [2.00] max.

Inch
[mm]

Tolerance Unless Noted			
	.0	.00	.000
inch	±.1	±.01	±.005

[ ] Dimensions for Reference Only

Ordering Information

102XX-0210EC

Contact Quantity
(See Table)

Application tools: 10951 Assembly Press and 10952 Cable Cutter.

3M
Interconnect Solutions
http://www.3M.com/interconnects/

For technical, sales or ordering information call
800-225-5373

Miscellaneous, Scratch, and Superseded Documentation

Microbolometer Setup Instructions

14 Nov 2013

1, Cable setups are on sheets with the cable.

2, The camera is a Photon 320

3, The VHDL ~~produc~~ project to use is 320_ethernet

4, The FPGA board to use is the ML-505.

5, The bitstream file to use is already present in the 320_ethernet directory. Programming instructions are with the project documentation

6, The ethernet driver does not work.

7, A ~~ca~~ Camera Link cable is used to connect the FPGA to the computer framegrabber.

8, The output is 324 columns x 256 rows x 14 bits

9, Use MatLab 7.11 R2010b SP2 32 bit version

10, Connect to the camera the cable labeled "Photon 320 camera"

11, ~~Ca~~ Connect the FPGA to the ~~cam~~ Camera Link cable using the ~~cable~~ cable labeled "Photon 320 Camera Link"

Photon 320 Cameralink Cable Pinout

12 Nov 2013

~~Break~~
Connector headers go in the differential column of J4 on the ML506 board

Twisted Pair Colors	Wire 1/Pin 1	Wire 2/Pin 2	Notes
Red, White	White/18	Red/20	Arrow at pos 20
Green, Red	Red/22	Green/24	Arrow at pos 24
Yellow, Brown	Brown/26	Yellow/28	Arrow at pos 28
Pink, Black	Black/30	Pink/32	Arrow at pos 32
Brown, White	White/34	Brown/36	Arrow at pos 36

To use, choose a wire pair listed in column 1. Plug in the connector such that the arrow is at the position located in column 4. The individual wires should then be connected as shown in columns 2 and 3.

Addendum Photon 320 Breakout Cable

Plug in the ~~brea~~ Photon 320 breakout cable such that the wires are connected to the differential column of J4, with the part marked "21" connected to pin 2 and the other pins in increasing order.

Connection	Wire #	Header Group	Header Pin	FPGA Pin (ML402)	FPGA Pin (ML506)
Synchronization -	12	~~J5~~ J4 on ML506	22	Y18	T34
Synchronization +	2		24	AA18	U33
CLK -	11		26	W19	U31
CLK +	7		28	Y19	U32
Data -	13		30	Y21	V33
Data +	8		32	Y20	V32

Header Pin name	Header Pin	Net Name
HDR2_22_SM_[illegible]_N	22	pcData0N
HDR2_24_SM_11_P	24	pcData0P
HDR2_26_SM_11_N	26	pcData1P
HDR2_28_SM_11_P	28	pcData0[illegible]
HDR2_30_DIFF_3_N	30	[illegible]
HDR2_32_DIFF_3_P	32	[illegible]

Pin 6 analog vid ~~[illegible]~~ -
Pin 1 analog vids +

P32		HDR2_12_DIFF_[illegible]_P	12	Idat
N32		HDR2_10_DIFF_[illegible]_N	10	IBdat
L34		HDR2_4_SM_2_P	4	isy
K34		HDR2_2_SM_[illegible]_N	2	ibs
K33		HDR2_8_SM_7_P	8	
K32		HDR2_6_SM_7_~~N~~	6	ib

Gnd 3, 4, 5,
Power 1.5, 10

TX 9 - ~~B~~DB9 Female 2
RX 14 - DB9 3

Header Pin	Net Name
2	ibs
4	isy
6	ib
8	i
10	Idat
12	IBdat

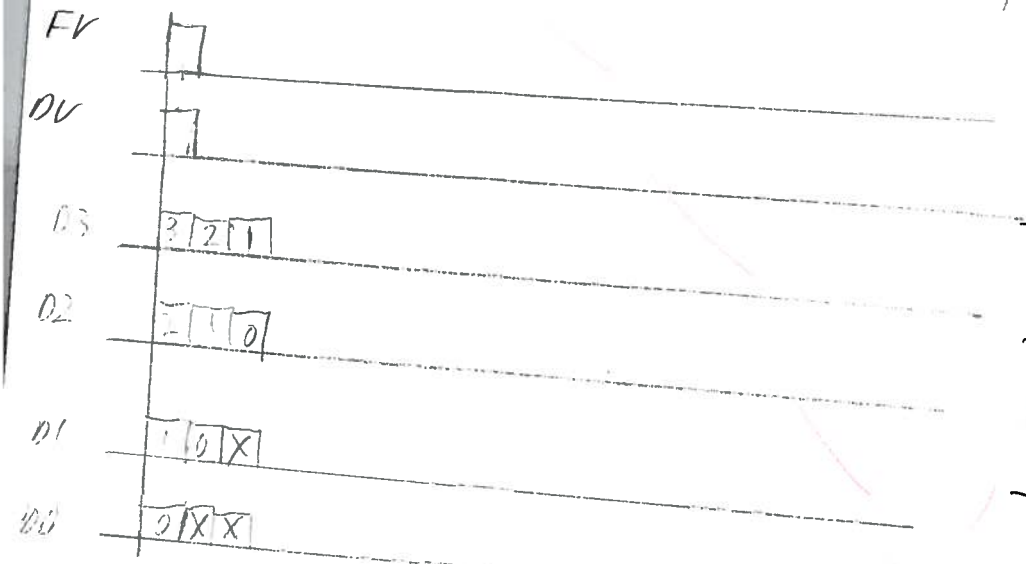
~~DTE~~
?? DTE Tx Pin 3
RX Pin 2

FPGA is DCE Wired

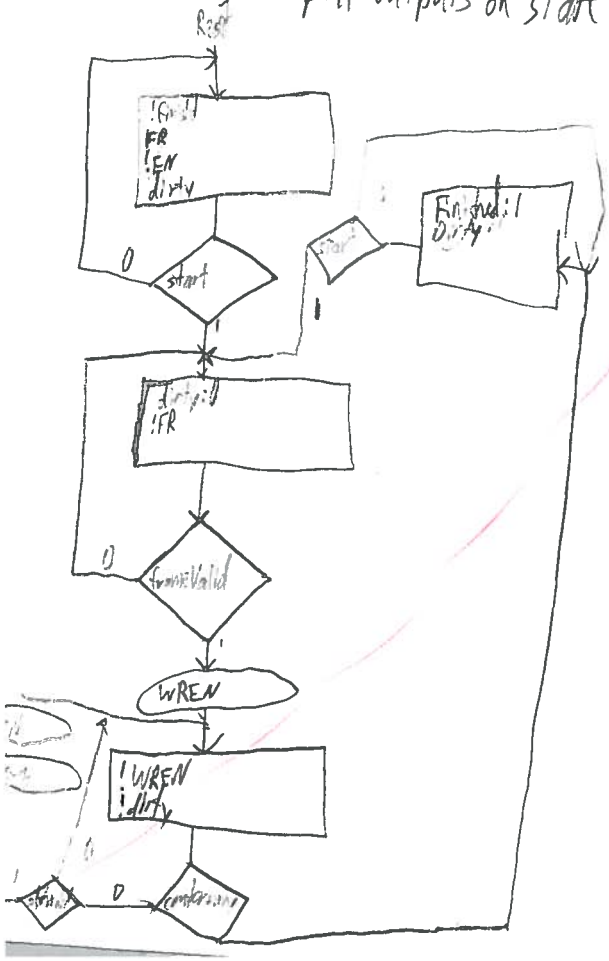
Docs say null modem cable needed for computer serial link, but comps are generally DTE, not DCE
Schematic says DTE, and has pin 2 hooked up to RX, and pin labeled as in.

FIFO=<x> means x is written to the FIFO

WREN is a Mealy output. Counter is incremented in a Mealy way



Change ~~output~~ outputs on state transition from C to A



Entity
- cam_clk in
- cam_data in
- start in
- resetn in
- data_valid buffer
- frame valid buffer
- ~~write_e~~
- write_en out
- dirty out
- finished out
- resetn out out
- deser_data buffer std_logic_vector(15 DOWNTO 0

Clk-	5	R32	TD_LITTLY_SMALL	18	HDR2_18_LITTLE_ENDIAN
clk+	18	R33	TOALITTLE_SMALL	20	HDR2_20_DIFF_ENDIAN
X0-	2	734	TOALITTLOPSMALL	22	HDR2_22_SMALL_ENDIAN
X0+	15	U33	TOALITTLOPSMALL	24	HDR2_24_SMALL_ENDIAN
X1-	3	U31		26	HDR2_26_SMALL_ENDIAN
X1+	16	U32		28	HDR2_28_SMALL_ENDIAN
X2-	4	~~U33~~ U33		30	
X2+	17	~~P33~~ U32		32	
X3-	6	V34		34	
X3+	19	W34		36	

Supported