INVESTIGATION OF SUPPORTING HARDWARE AND PIXEL DESIGN FOR PHOTON-NUMBER-RESOLVING IMAGERS

by

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Abstract

This project consists of two significant parts. First, the cryogenic supporting hardware for a Quanta Image Sensor (QIS) is optimized and fabricated. The second part is a pinned photodiode (PPD) transient simulation in TCAD software. The hardware needed to operate a QIS device within a low-temperature environment must simultaneously support high-speed digital signals and sensitive analog signals. The initial hardware design is adapted from a prototype developed in the lab of Professor Eric Fossum at Dartmouth. The printed circuit board (PCB), referred to as the Cold Electronics Board (CEB), is redesigned in Eagle. The system design is optimized for power and grounding performance for later routing and fabrication. Multiple grounding techniques are considered, and a star-ground is chosen. Further, the performance of one power supply is theoretically compared to that of an additional power supply. Secondly, an Indium-Gallium-Arsenide (InGaAs) Pinned Photodiode (PPD) is modeled to estimate transient operation. The InGaAs stoichiometry is chosen to detect 1550 nm light optimally. Synopsys Sentaurus TCAD is used to simulate both the steady-state and transient operation of the PPD, with an existing two-dimensional PPD project serving as the basis of the project. The device is 1.5 μm wide, and the substrate is 5 μm thick. Sentaurus Device is used to create a simulation profile to perform a transient analysis of the PPD. This simulated measurement techniques can be applied to different systems with a similar structure in both 2D and 3D.

Acknowledgment

I am very grateful to Professor Figer, my advisor, for providing me with the opportunity to work in the RIT Photonics lab. His support made this project possible. I am honored to have been able to work with a renowned researcher in imaging science, and appreciative that I was trusted to work on large funded projects within the lab and offered exciting research to explore. I have gained lots of hands-on experience in a field that I previously found inaccessible. Further, without the work done in this lab group, I would not have had the chance to learn as much as I did in such a short period of time. The work I completed here instilled a great amount of interest in this field. I am also grateful to Justin Gallagher for his extended support and guidance throughout my involvement in the lab. His responsive and helpful nature enabled me to get up to speed with all of the lab systems and past work. I would also like to thank everyone within the Photonics lab for onboarding me and putting me to work amidst the struggle of the pandemic.

I also thank post-doctoral researcher George Nelson of NPRL for helping me navigate the latter half of my project. His vast knowledge of semiconductor devices was incredibly helpful as he taught me relevant topics and material to aid in my understanding of the project. Further, his support in TCAD enabled me to understand not only how to use the tool but the math behind them as well.

Lastly, I thank my parents for their support of my academic pursuits. Their words of encouragement, edits, and patience helped me persevere through a difficult, remote time and complete this work.

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1 Introduction

Image sensor technology has had a significant cultural impact. These devices influence many areas of life, from social interaction and photography to scientific discovery and exploration. In 1997, Dr. Eric Fossum published a paper describing a CMOS image sensor [1], initially designed for NASA missions. This invention marks the beginning of an explosion in the development of practical imaging. CMOS image sensor technology has become ubiquitous. Now, the devices have advanced so far that the devices are pushed to their physical limits. Some advanced research has taken the form of single-photon resolving imagers. These devices can capture images in ultra-low light settings. Modern photon number resolving devices using CMOS technology has been pioneered by Fossum [2]. Fossum refers to these devices as Quanta Image Sensors (QIS), and this term will be used in this report. Sensors that can detect such small signals have many essential use cases, such as vastly improved low light imaging and research in photonics. Hence, photon number resolving imagers have been heavily investigated.

This project investigates the performance of the supporting hardware of a Quanta Image Sensor and develops an Indium-Gallium-Arsenide (InGaAs) photodiode. The first section of this report covers the optimization and manufacturing of the electronics required to operate a QIS device. The second section presents a model designed to estimate the transient action of photodiode structures in Synopsys Sentaurus TCAD. This report will start with an introduction to the relevant topics in detection.

2 Background

2.1 Photodetectors

Photodetectors record the presence and intensity of incident light. Methods and devices for photodetection have taken many forms throughout history. Modern light-sensing techniques are primarily implemented with semiconductor technology, referred to as solid-state photodetectors. These devices typically take advantage of the photovoltaic effect to convert light to electric current. This review will discuss the history of photodetectors and provide an overview of relevant devices, solid-state and otherwise.

2.1.1 Historical Review of Solid-State Photodetectors

Before the use of solid-state photodetectors, the study of many other photosensitive materials took place. A familiar example is the flexible photosensitive film in film cameras, pioneered by Eastman in 1888 [3]. Nishizawa introduced the first PIN photodiode in 1950, and Weckler reported the first PN junction photodiode in 1965 [4]. Soon after, the charge-coupled device (CCD) was presented by Boyle and Smith in 1969 [5] as a memory device. The use of CCDs for photodetection was quickly apparent, leading to research for their application in imaging [5]. The first digital camera was developed at Eastman Kodak by Steven Sasson in 1975 [6] using a CCD device designed by Fairchild Semiconductor. This camera weighed 8 pounds and could capture images with a resolution of 0.01 megapixels. In the following decades, advances in CCD technology, solid-state memory, and data compression enabled more practical digital cameras.

Cameras using CCD technology remained the primary focus of solid-state imager development until Fossum published the CMOS Active Pixel Sensor (APS) in 1997 [1]. Active

pixel sensors have many advantages over CCDs. The rapid development of Silicon CMOS processes in the late 1990s and early 2000s enabled commercially available APS devices. Riding the wave of Moore's law, CMOS photodetectors quickly advanced and became ubiquitous throughout the consumer space. State-of-the-art consumer devices have surpassed 100-megapixel resolutions, one-thousand times higher than the Kodak camera of 1975. With the shrinking of CMOS technology, pixels in modern cameras include more advanced circuitry [7]. Devices using this technique are commonly referred to as smart CMOS image sensors [7]. Smart CMOS devices can include multiple photoelectron storage sites [8] and machine learning integration [9], among other possibilities. Modern transistor manufacturing processes have enabled the miniaturization of imagers for use in space-constrained applications. Shrinking the size of the active area of a pixel changes the properties of the device. The use of signal processing and specialized optics can further tailor devices to individual applications. CMOS photodetector technology has matured into a stable and practical technology.

Now, the industry is on the edge of a new era of photodetectors. Imaging research is branching into new approaches to detection. Notably, Fossum has contributed to the development of photon-counting CMOS imagers, referring to them as Quanta Image Sensors (QIS) [2]. As defined by Fossum, QIS devices are arrays of photon-number-resolving pixels. As the name suggests, photon-number-resolving devices count light quanta or photons. A photon is a particle of light, representing the least detectable quantity of light energy. Previously, manufacturing techniques have prohibited such ultra-sensitive devices from being implemented in low-cost silicon processes. As shown, semiconductor process advancements and research in pixel design have yielded devices capable of detecting countable numbers of photons at a pixel level. Room-

temperature QIS devices have already been demonstrated to have photoelectron counting capability [10].

2.1.2 Passive PN Photodiode

A PN Photodiode is the simplest form of a solid-state photodetector. The device is composed of two oppositely doped and physically adjacent regions in a semiconductor substrate designed to react to incident light. The two doped regions yield a gradient from one carrier concentration to another. The gradient between the two doped regions is referred to as the depletion region. An example I-V curve is shown in Figure 1. Incident photons hit the material, generating electron-hole pairs. If the diode is connected to a load, the carriers will leave the diode and travel through the load to complete the circuit. Alternatively, light can be detected by applying a reverse bias to the diode. The reverse bias will widen the depletion region, even after the bias is removed. Once in this state, incident light will create carrier pairs that will meet in the depletion region and reduce its width, causing a detectable change in potential across the device. This effect will continue until the depletion region has reached equilibrium, otherwise known as saturation. PN photodiodes are simple to manufacture and are widely available in many configurations.

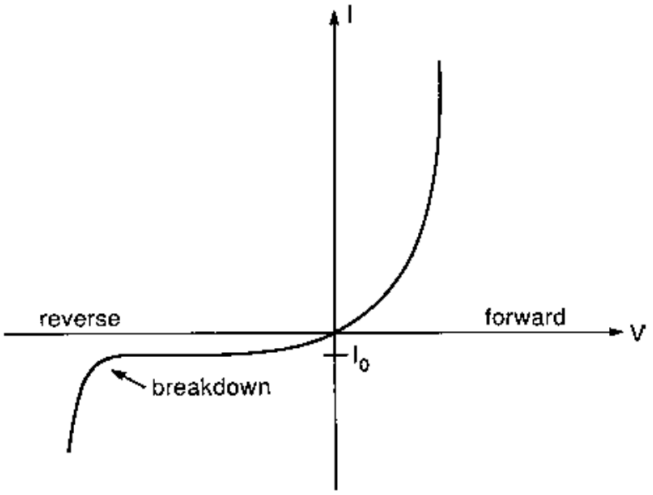

Figure 1: Generic photodiode I-V (current-voltage) curve from [11].

2.1.3 Active Pinned Photodiode

A pinned photodiode (PPD) is a type of buried photodiode. A PPD is composed of a p doped substrate, large n-type storage well (SW), a p+ pinning layer, a transfer gate, and an n+ floating diffusion region. The output region is also referred to as the floating diffusion region (FD) [12]. Figure 2 is a capture of a two-dimensional PPD simulation, which represents the cross-section of an implementable device. The PPD is operated using readout electronics. An example of the readout configuration is shown in Figure 3. This example uses four transistors: transfer (X_i), reset, output or source follower (D_{ij}), and word. The four-transistor (4-T) configuration is standard in modern CMOS image sensors.

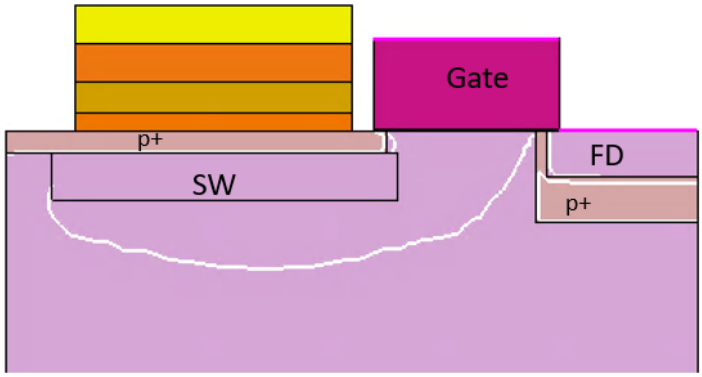

Figure 2: PPD diagram captured from Sentaurus simulation with labeled regions.

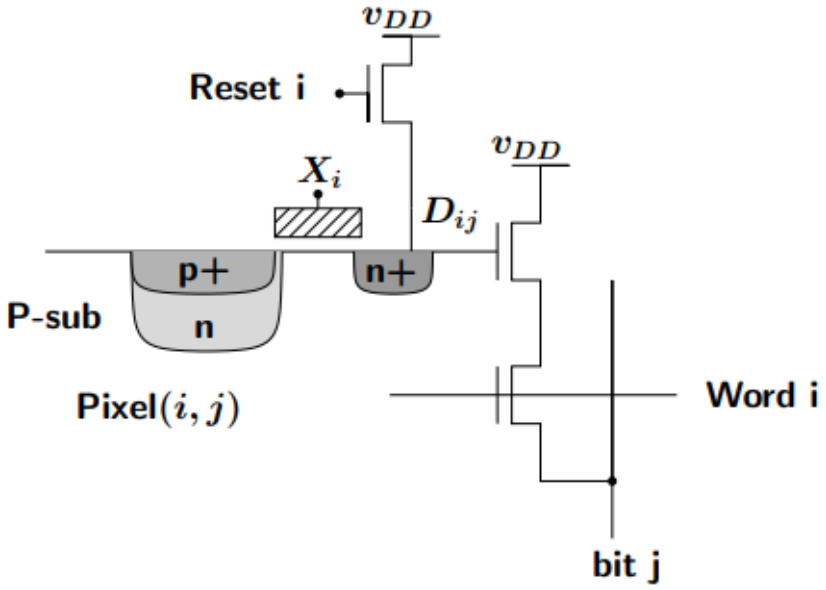

Figure 3: A generic diagram of a four-transistor pinned photodiode (4T PPD) from [13]. Note that X_i corresponds to the transfer gate of the photodiode and counts as one of the 4T.

The operation of such a pinned photodiode is primarily through the control of the transfer gate and the reset gate. This operation is shown in Figure 4. The reset gate is pulsed to set, or pin, the charge in the FD region to a known value. The transfer gate is activated after the falling edge

of the reset pulse. The transfer gate lowers the potential barrier between the SW and the FD, allowing the electrons that are collected in the SW to flow to the FD. The signal is determined by comparing the charge in FD after reset and after the transfer of charge. Typically, the FD will be connected to a source follower transistor, shown as D_{ij} in Figure 3. In this configuration, the charge accumulation in FD is not destroyed or perturbed, and multiple measurements can be made.

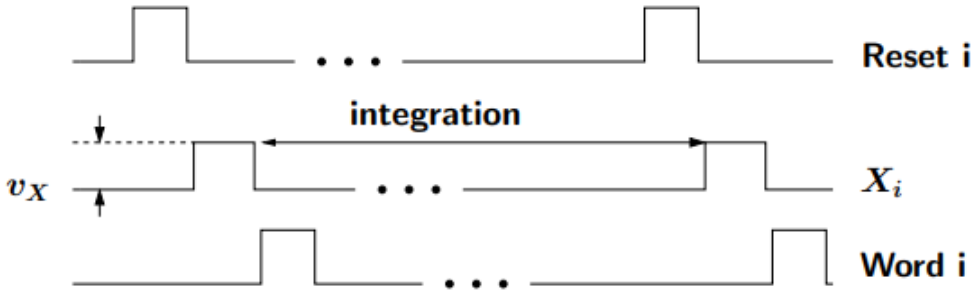

Figure 4: A generic PPD operation timing diagram from [13]. The Gates labeled in this diagram correspond to the gates in Figure 3. After each integration, the FD is reset, the charge is transferred from the storage well, and the word transistor enables the source follower to output a signal.

2.1.4 Semiconductor Materials for Photodetectors

Typically, semiconductor devices are made from Silicon (Si). Si is by far the most used semiconductor material due to its abundance on Earth and many desirable features for electronic integrated circuit (IC) manufacturing. Many modern photodetectors are composed of Si because detectors made of this element can capture light from the visible spectrum, making it widely useful. However, different materials must be used to detect wavelengths that Si detectors effectively cannot capture due to the bandgap of Si.

Through the photovoltaic effect, semiconductor devices transform light energy into electrical charge [14]. Incident photons penetrate the surface of the semiconductor material and strike the atoms in the crystal lattice. This energy is transferred to an electron. With sufficient energy, the electron can move from a valance band position in the lattice to a free position in the conduction band. This barrier between the valence band and the conduction band is called the bandgap. The bandgap varies between different semiconductor materials. One can take advantage of this variation by growing alternative crystal substrates to make detectors for almost any desired wavelength. Figure 5 demonstrates this effect. Each point represents the bandgap of the marked material. The solid lines represent different bandgaps that can be achieved by varying the stoichiometry of a combined crystal. In other words, the ratio of two or more materials can be varied to fine-tune the desired bandgap and further the target wavelength.

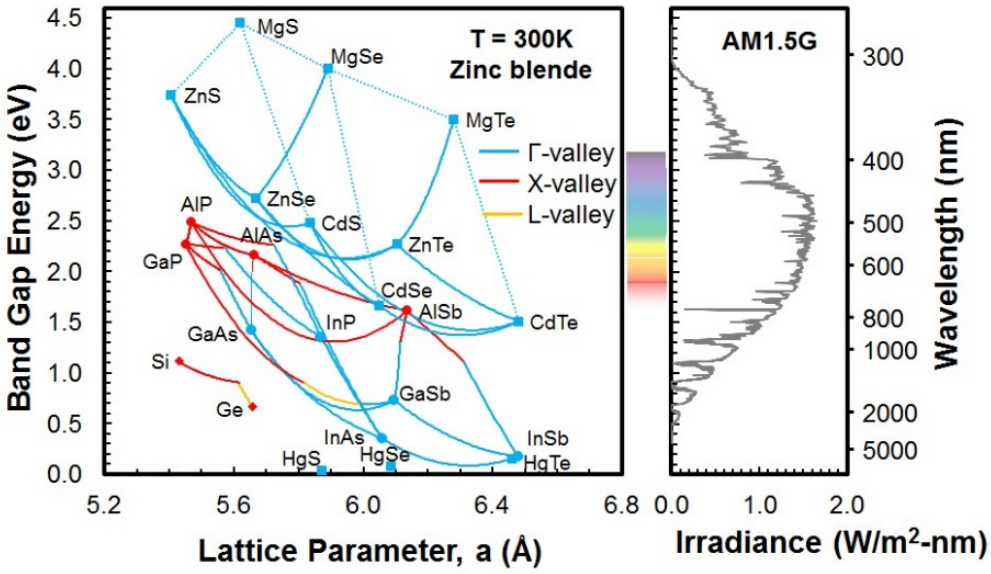

Figure 5: A plot of bandgap vs. lattice constant, from [15]. Various InGaAs stoichiometries are represented by the line that connects GaAs and InAs on the left plot.

Due to the fabrication complexity of some materials, many non-silicon devices are not monolithic. In many cases, such as InGaAs in this project, the required fabrication technology does not exist to create a monolithic device either reliably or cost-effectively. Many systems with III-V (or more exotic) devices opt to use the flip-chip bonding technique to connect devices fabricated with different materials to solve this problem. This technique is also referred to as a controlled collapse chip connection (C4). Conductive bumps are deposited on metalized regions on the top of the chip to be attached. The chip is then flipped so that the conductive bumps line up with metal regions on the receiving chip. The connection is made by remelting the conductive bumps with hot air reflow.

Flip-chip bonded integrated circuits (flip-chips) have the advantage of using specialized materials for specific circuits, such as pixels, while reducing the cost by implementing the remainder of the circuitry in Si, such as the readout system. A typical application of the flip-chip technique is the bonding of a pixel array to a readout integrated circuit (ROIC). There are some drawbacks, however. In comparison to monolithic implementations, flip-chips are noisier, less durable, and require more processing. Flip-chips are usually the only option when working with specialized materials because fabricating the entire IC in such a material is typically more expensive, less reliable, or entirely impossible.

2.1.5 Practical Comparison of CCD and CMOS Architectures

Charge-coupled devices (CCD) were the first devices to be reliably used as solid-state imagers. CCDs are sequentially addressable arrays of intrinsic photodetectors [11]. When cooled, CCDs can reach fundamental detection limits for most wavelengths between approximately 1 nm and 1 μm [11]. Advanced CCD applications such as electron-multiplying CCDs (EMCCDs)

enable higher sensitivity through the use of electron-multiplying registers. EMCCDs can achieve gain levels up to one thousand times higher than traditional CCDs, making them ideal for photon counting. However, CCDs are limited in high-speed applications and require multiple high voltage power supplies for the readout analog circuitry. Further, the CCD imager readout is destructive, i.e., the signal is not recoverable after each readout.

Complementary metal-oxide-device (CMOS) image sensors (CIS) are an alternative to CCD devices. CMOS imagers are arrays of individually addressable active pixels. In consumer electronics, silicon CMOS is the most common imager technology due to its low cost and high performance. The vast progress of the CMOS manufacturing processes has played a role in the capabilities of modern CIS chips. CMOS imagers use digital circuitry that is smaller and more power-efficient than a CCD alternative. Additionally, smart readout electronics can be integrated within each pixel. Each pixel may have a different noise level per the manufacturing variation in the amplifiers, but the advanced CMOS process has mitigated this issue.

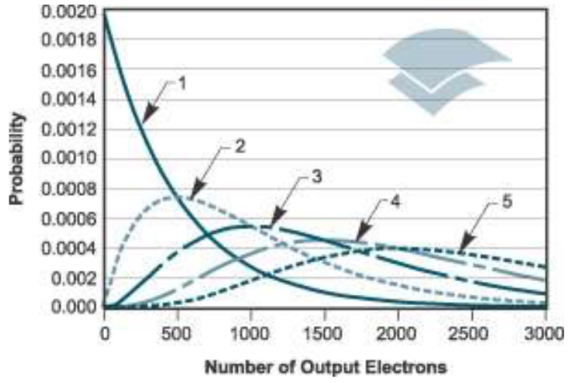

Figure 6: A photon number probability vs number of electrons plot from an EMCCD set to a gain of 500 from [16]. The number of photons counted is determined by finding the maximum probability for the number of electrons counted.

2.1.6 Photon Counting

In contrast to typical image sensors, photon-resolving devices detect individual or small numbers of photons. Typically, a pulse is emitted for each photon, allowing for electronic photon counting. Such devices help capture signals in specialized settings such as low light, telecom, and scientific research. However, due to the high sensitivity, the maximum detectable signal of photon-resolving devices is relatively low compared to typical photodetectors.

The photoelectric effect was first observed by Heinrich Hertz in 1887 [16] and explained by the theory of Albert Einstein in 1905 [14]. The photoelectric effect is the phenomenon in which electrons are emitted from a material that is exposed to light. The electrons released in this way are referred to as photoelectrons. Naturally, this effect is helpful to measure light with existing electronic sensing techniques. In conjunction with the suggestion of light quanta, the motivation to design a device to detect a minimum light intensity event, a single photon, is clear.

Early photon counting devices were modifications of radiation detection systems. For example, Elster and Geitel [17] created a photoelectron detector inspired by the concept of the alpha particle detector by Rutherford and Geiger in 1908 [18]. The device is a gas-filled bulb with photoelectric material inside and a metal cathode and anode extending outside the bulb for detection. A photon enters the bulb and strikes the photoelectric material. The generated photoelectron then causes a detectable discharge via the ionization of the gas. These devices were noisy and relied on sensitive electron detection.

Later, photomultiplier tubes (PMTs) solved the problem of detection. PMTs are vacuum tubes that use dynodes to achieve electron multiplication via secondary emission, effectively returning multiple electrons for a single photoelectron. There is some contention regarding the

original invention of the PMT [19]. Slepian created the first PMT in 1936 using 12 dynode stages to achieve high gain [16]. Research on the improvement and miniaturization of PMTs continued for many decades, and the devices are still manufactured today. The avalanche photodiode, invented in 1953 by Nishizawa in 1952 [20], is a semiconductor analog to the PMT.

Avalanche photodiodes (APDs) are solid-state devices that conceptually work similarly to photomultiplier tubes. An APD is a highly sensitive photodiode that takes advantage of the photoelectric effect and avalanche breakdown to release many electrons for each incident photon. Avalanche breakdown in semiconductors occurs when carriers are accelerated to the level at which they can create additional electron-hole pairs via collisions. This effect is observed in diodes constructed to break down at a significant reverse bias. As solid-state device technology matured, other devices, such as the charge-coupled device (CCD), were explored for photon-counting applications.

The CCD discussed above was introduced by Boyle and Smith in 1965 [5]. The first CCD devices generated far too much noise to detect individual photons. Early photon-counting CCD systems used image intensifiers to amplify the incoming signal for detection [16]. Developed for early television cameras, image intensifiers included various technologies to amplify an optical signal before a detector. Later, developments in CCD technology allowed for the use of CCD sensors for photon counting directly, such as the low light level charge-coupled device (L3CCD) [21]. Sampling techniques such as correlated double-sampling (CDS) [22] allow for readings with lower noise than direct measurement and are still used to improve performance today. Recently, advances in CMOS image sensor technology have enabled CMOS imager structures for photon-counting [2].

2.1.7 State-of-the-Art Photon-Resolving Image Sensors

The development of image sensors capable of detecting individual photons has continued. As of the writing of this report, the most advanced CMOS photon resolving image sensor boasts a 16.7-megapixel resolution and includes a programmable analog-to-digital converter (ADC) for data processing [23]. This device was designed by Gigajot® in Pasadena and described in a publication in 2021 [24]. A Gigajot® prototype device is the center of the supporting hardware design discussed in this report. The development of these devices will likely continue, leading to overall improvements, such as higher resolutions and lower noise values.

3 Supporting Hardware Optimization

This section is a discussion of the optimization of the supporting hardware designed for a photon-resolving imager. The photon resolving image sensor was provided by the lab of Dr. Fossum at Thayer School of Engineering at Dartmouth. The device is a prototype of the Gigajot® Pathfinder device and will be referred to as the Quanta Image Sensor (QIS). The project that includes both RIT and Dartmouth is funded by the Strategic Astrophysics Technology (SAT) program of NASA. This project, led by Justin Gallagher, M.S., and Donald Figer, Ph.D., is ongoing and aims to improve the readiness of single-photon resolving imagers for future use in NASA missions. The role of this supplemental report was to analyze the desired system and provide advice and design direction to enhance the performance of the QIS supporting circuitry used for characterization and later experimentation. All of the following analyses and recommendations were completed and provided before the routing and manufacturing of the final system.

3.1 Overview and Constraints of the System

The overall camera system is composed of three main parts: the warm electronics box, the cold electronics board, and a photon resolving imager. The warm electronics box contains a field-programmable gate array (FPGA), interface cables, and power supplies. The cold electronics board (CEB) assists in the operation and readout of the QIS. This report consists of efforts to improve the CEB layout, overall power distribution, and system manufacturability.

3.1.1 Photon Resolving Imager or QIS

The QIS device used in this project is a prototype version of the Gigajot® Pathfinder device with ten digital and ten analog channels. For the QIS device to effectively count photons,

the read noise of each pixel must be significantly less than one electron (< 1 e^- r.m.s.) [25]. The QIS device is cooled to achieve the required read noise. In the case of this experiment, the QIS is operated at temperatures as low as 150 K. The pathfinder device uses a typical CMOS pixel architecture and can provide either digital or analog values depending on the readout configuration [25]. The system described here supports both readout methods, leading to a complex mixed-signal design.

3.1.2 Cold Electronics Board (CEB)

The role of the cold electronics board is to receive, process, and transmit the signal from the QIS device from inside a cooling Dewar. A rigid printed circuit board (PCB) holds the readout and transmission hardware, and a rigid-flex PCB holds the QIS with a matched socket. The CEB needed to meet the physical and operational constraints of the Dewar such as the chamber size and the low experimental temperature. The board was designed to fill the available space in the Dewar to maximize performance and aid in routing. The rigid-flex section was designed to allow the QIS device to be positioned for testing by meeting the constraints of the imager mount within the Dewar. The main board was implemented in four layers, the two rigid sections of the extension board in eight layers, and the flex section in three overlapping two-layer flat-flex connections.

Due to the analog and digital operating modes of the QIS, the CEB needed to be optimized to receive either type of signal, posing challenges in grounding, power, and part placement. The analog signals are more sensitive to noise and must be routed to an analog-to-digital converter (ADC) to avoid possible signal contamination. While the high-speed digital logic is more resilient than the analog signals, the logic signals must also be routed with care until converted to a more stable format for transmission to the FPGA. Low-voltage differential signaling (LVDS) was

implemented to transmit the image information from the CEB through the Dewar wall to the FPGA. LVDS is a high-speed and low-power transmission standard for binary data over a twisted pair of copper wires. LVDS was used because it can handle the speed of the required clock signals and offers a rejection of common-mode and ground noise [26].

3.1.3 Warm Electronics Box

The warm electronics box houses the FPGA controller and the power systems. A Xilinx KC705 FPGA development kit was employed. Graduate Researcher Irfan Punekar programmed the FPGA to transmit control signals and receive image data from the CEB.

Due to the complexity and sensitivity of the system, there were many constraints on the power systems. The power supply was required to transform and filter wall power (120V AC, 60Hz) to 12V power to the FPGA, the CEB, and by extension, the QIS device. Additional power-management electronics, such as power regulators on the CEB, were needed to power the QIS correctly. Noise was to be kept at a minimum to protect the sensitive signals on the CEB. The grounding scheme, and by extension, the power supply layout, is the subject of exploration in this report.

3.2 Grounding Scheme

The QIS system required a thoughtful grounding scheme due to the nature of the QIS device and its respective signals. It was essential for the supporting hardware to maintain both sensitive analog signals and high-speed digital signals while preventing the comingling of the two. The primary target of noise reduction was signal separation. Signal separation is desirable because it prevents interaction between sensitive signals in both transmission and return current. If signals

are allowed to impact each other, the undesired overlap manifests as noise. The single-point star grounding technique between the split digital and analog ground planes mitigates these noise sources. It is desirable for the power distribution to resemble the structure of the grounding scheme. By convention, the grounding scheme is designed first, and power distribution follows [27].

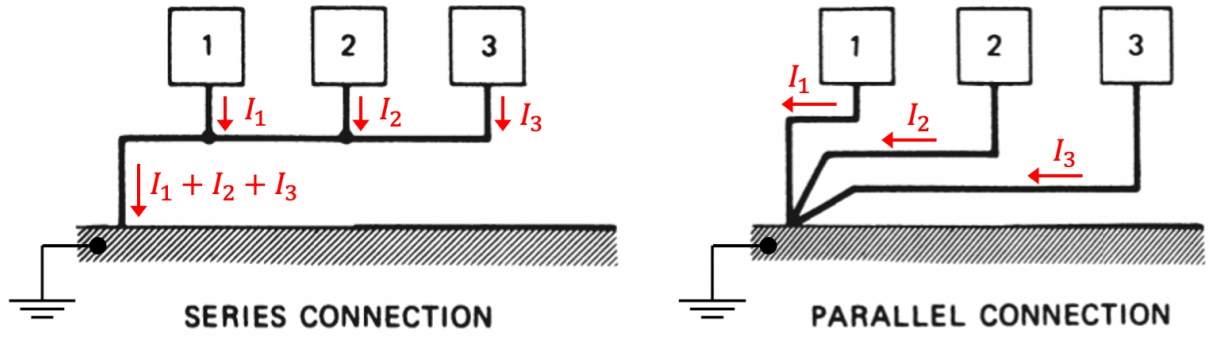

Figure 7: Comparison of series, parallel ground connections for three circuits, modified from [27].

Star grounding, or parallel grounding, can reduce the interaction of digital and analog signals and minimize grounding noise. As shown in Figure 7, star grounding is achieved by directly connecting individual circuits directly to ground. Series grounding is an alternative to star grounding in which circuits are connected on a shared ground path. In series grounding, the return current of multiple circuits are combined into a single trace, potentially causing crosstalk or noise caused by signal interaction. Star grounding comes with the advantage of reducing the crosstalk of each circuit by providing unique return paths. However, star grounding is typically more complex and more cumbersome to design. Further, single-point star grounding will effectively become multi-point grounding at high frequency (approx. >100kHz) due to parasitic series inductances and capacitance to the ground plane [27].

The CEB main board was designed with a split ground plane. The split ground plane helped prevent the high-speed digital logic from interfering with the sensitive analog circuitry. The physical gap between the ground planes prevented the return currents from comingling. The ground planes met at a common ground point to avoid creating a large ground loop through the entire system. The mixed-signal components were placed along with the split over a connection between the analog and digital to create a single ground connection between the two planes. The common ground point, or bridge, is placed underneath the mixed-signal components, such as the analog-to-digital converters. No traces were to be routed across this bridge to prevent the return path of a digital signal from disrupting the analog circuits. Within each ground plane, the components connect directly to their respective ground plane. This is referred to as multi-point grounding.

Once the grounding scheme was designed, the power distribution was employed in a similar fashion. It is possible to disrupt a well-conceived grounding design with a poor power distribution plan, so both were treated with care.

3.3 Power Supply Optimization

Power distribution for the system was optimized to reduce noise, increase reliability, and improve the protection of the sensitive QIS. Multiple power supply schemes could effectively power this system, but thoughtful design improved the overall performance.

Three design choices were considered: one, two, or three separate power supplies. Each power supply transforms AC wall power into 12V DC power. Wall power was routed to each power supply via a power entry module. Initially, all power supplies were to have a dedicated

power entry module. The final version of the QIS evaluation system includes three power supplies to minimize changes between the new design and the original Dartmouth hardware. Once the number of power supplies was chosen, the number of power entry modules was discussed. One power entry module is used to minimize noise.

3.3.1 Three Power Supplies

In a possible three-power-supply configuration, each major circuit group receives separate power. The digital side of the CEB, the analog side of the CEB, and the FPGA all have a dedicated power supply, as shown in Figure 8.

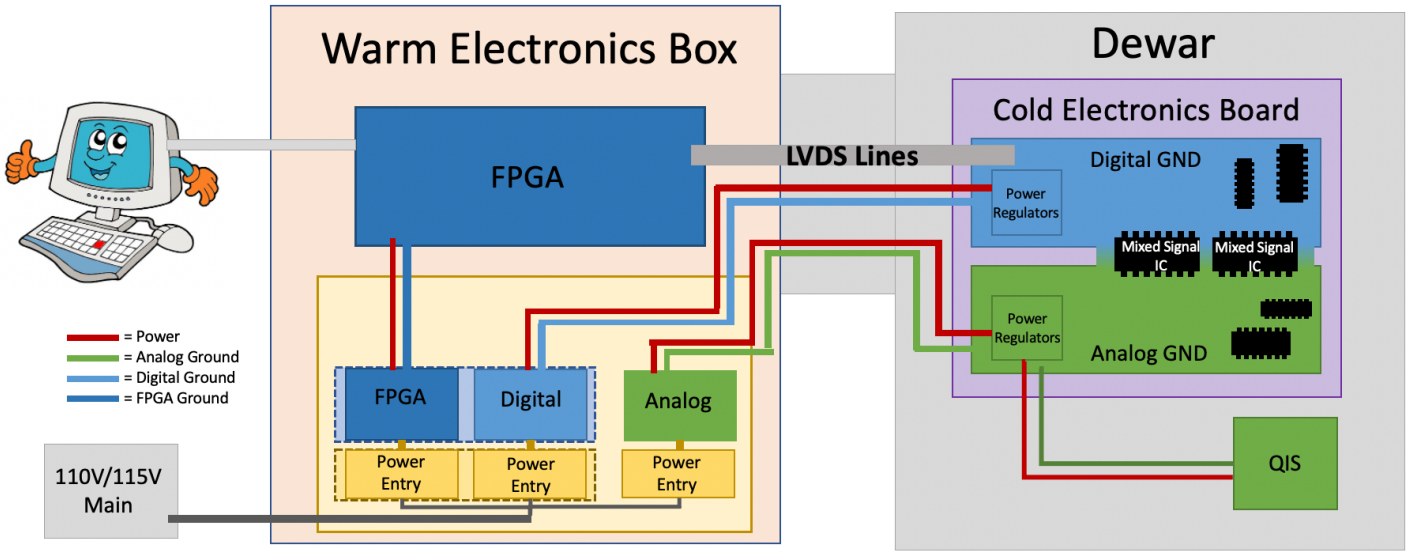

Figure 8: System overview using two or three power supplies. The dotted lines indicate blocks that could potentially be combined to reduce the system to two power supplies.

This power supply configuration allows for signal separation by providing a discrete power supply and return path for each major circuit group. Physically isolating the power supplies aids in preventing crosstalk, but this benefit evaporates without proper consideration. With the optimal layout, the return path of each circuit group does not find its way to the ground path of an opposing

power supply. However, due to the previously imposed design of a ground bridge between digital and analog ground, this power supply configuration opens the door to large ground loops.

As previously noted, the analog and digital grounds on the main board of the CEB are connected via a bridge. If a trace originates from a digital device and terminates on the analog ground, two undesirable situations can occur. If the digital signal is high frequency, current will flow underneath the digital trace back to its origin and to the digital supply ground. The path directly underneath a high-speed trace is followed because it is the path of least impedance, and in this case, least inductance. The current flowing underneath the digital trace will partly flow into the analog ground, interfering with the sensitive analog signals. If the digital signal is low frequency, the return path is instead through the analog supply ground, eventually returning to the common ground of the power supplies. The low-frequency return path introduces more noise than the high-frequency case because the digital signal is directly mingling with the analog signals by sharing the same current return. In this case, it is also easy to identify a large ground loop from the digital supply ground to the digital ground, through the analog ground, and back through the analog supply ground.

Additionally, the digital side of the CEB and the FPGA are connected directly and communicate using the LVDS protocol. Systems using differential signaling require a ground connection at a common level on either end. If a separation between ground levels becomes too large, the LVDS receivers will no longer detect the incoming information, and the transceivers risk permanent damage. LVDS signal swing is 400 mV with a typical common mode voltage of 1.2V [27]. Standard receivers can tolerate up to a $\pm$1V ground shift from the ground of the transmitter [27]. Beyond this, signal may be lost. The use of two independent power supplies for each circuit

group increases the risk of this scenario. The ground level of isolated power supplies can gradually shift during operation. Further, anomalous activity on power lines can cause relatively large and abrupt power and ground changes. Also, the LVDS traces on the CEB and FPGA can create a ground current directly underneath them within their respective ground planes due to the present fields. As long as the traces are routed properly, however, this effect should have minimal effect on noise.

The configuration employing three power supplies with independent power entry modules was determined to be unnecessarily complex and was not selected. Reducing the number of power supplies and entry modules to two or one mitigates the design challenges discussed above.

3.3.2 Two Power Supplies

A two-power-supply configuration separates the system into analog and digital power. The analog supply would cover the QIS and the analog components on the CEB. The digital supply would power the digital side of the CEB and the FPGA. This configuration is represented in Figure 8 by effectively combining the digital and FPGA power supplies, as indicated by the dotted lines. The grounding of the two power supplies would meet under the mixed-signal components on the CEB in a single-point star ground.

The two-power-supply option would enable the design of separated return paths of the digital and analog circuits, similar to the three-power-supply option. Additionally, the reduction to two power supplies mitigates the risk of supply and ground drift between the FPGA and CEB. Using two power supplies also would reduce the cost and complexity of the overall system.

3.3.3 One Power Supply (Suggested Improvement)

The simplification of the power design to a single power supply suggests improvement over the two-power-supply and three-power-supply configurations. One power supply fed by a single power entry unit would be used to power the entire system. The grounding scheme would remain a single-point star ground for the entire CEB and multi-point ground for each ground plane. All of the ground routings would emanate from the star ground, with the exception of the FPGA. Further, the power lines would follow a similar path.

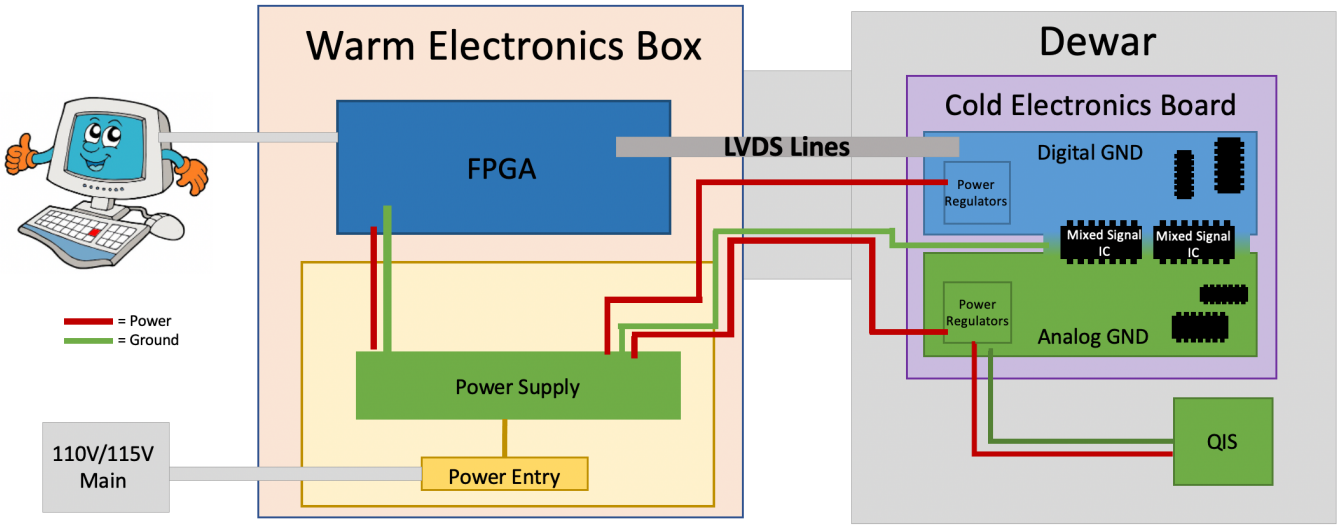

Figure 9: Proposed single power supply configuration

The star grounding remains to aid in isolating the analog and digital circuits with one power supply. Additionally, the single ground source eliminates the risk from ground loops and voltage level drift imposed by multiple power supplies. The FPGA would receive a separate ground connection from the CEB because it is isolated by differential signaling. In the future, the isolation can be improved by the use of optical data transmission.

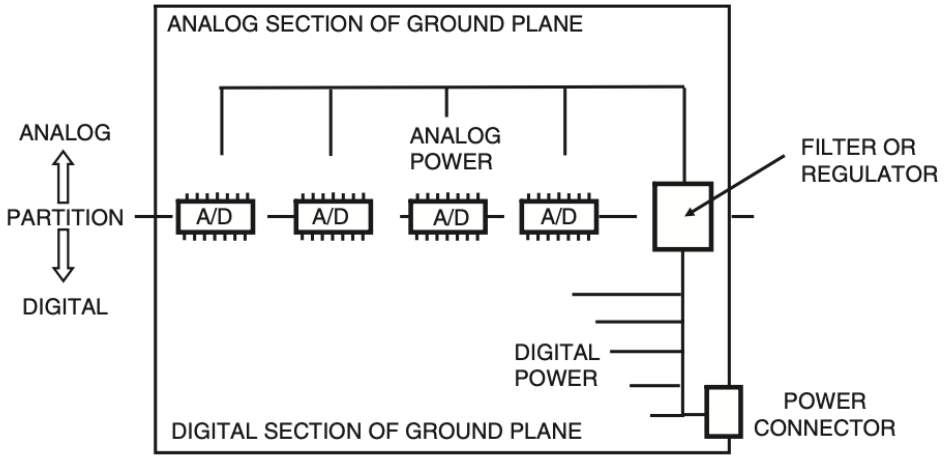

Figure 10: Proper mixed-signal PCB power distribution from a single supply (from [27]).

In a multi-power-supply configuration, independent PSUs provide source isolation. It is possible to achieve excellent isolation with one power supply with a thoughtful design. Voltage regulators provide a reasonable degree of isolation by protecting circuits from power supply noise. The power supply ripple rejection (PSRR) is reported in the datasheet of most voltage regulators. Regulators that meet the required noise rejection can be identified by comparing PSRR values. An generic example of a well-laid-out mixed-signal PCB is shown in Figure 10.

Further, regularly placed decoupling caps and ferrite beads help decouple circuits from noise on the power lines by providing low impedance paths to ground. On mixed-signal components, decoupling capacitors must be connected from a supply line directly to the digital ground pin. If the frequency of the digital noise is known and well understood, filters can be implemented to reduce or remove the noise from the power rails before the analog components use them.

3.3.4 Reduction of Power Entry Modules

The team opted for the use of three power supplies with one power entry module to most closely resemble the power distribution of the original Dartmouth design (in which two discrete benchtop power supplies are used to power the equivalent of the CEB). The team implemented this design after the conclusion of this supplemental project. The system is configured to operate with one, two, or three power supplies for testing. However, the primary operating mode is with three power supplies.

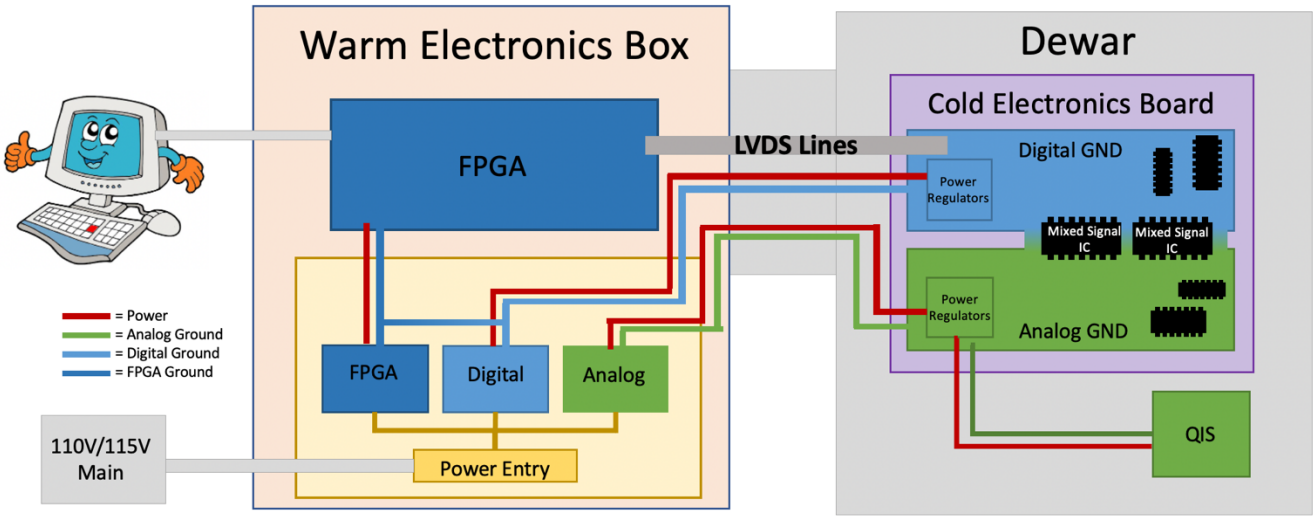

Figure 11: Final configuration of the CEB for testing.

3.4 Rigid-Flex QIS Receptacle Board

A rigid-flex extension of the CEB is designed and built for more flexible positioning of the QIS inside the Dewar. The PCB has two eight-layer rigid sections connected by three overlapping two-layer flat-flex sections. The first rigid section connects to the CEB with three connectors, and the second receives QIS with a chip receptacle. The flat-flex section is separated into three separate two-layer stirps to improve flexibility.

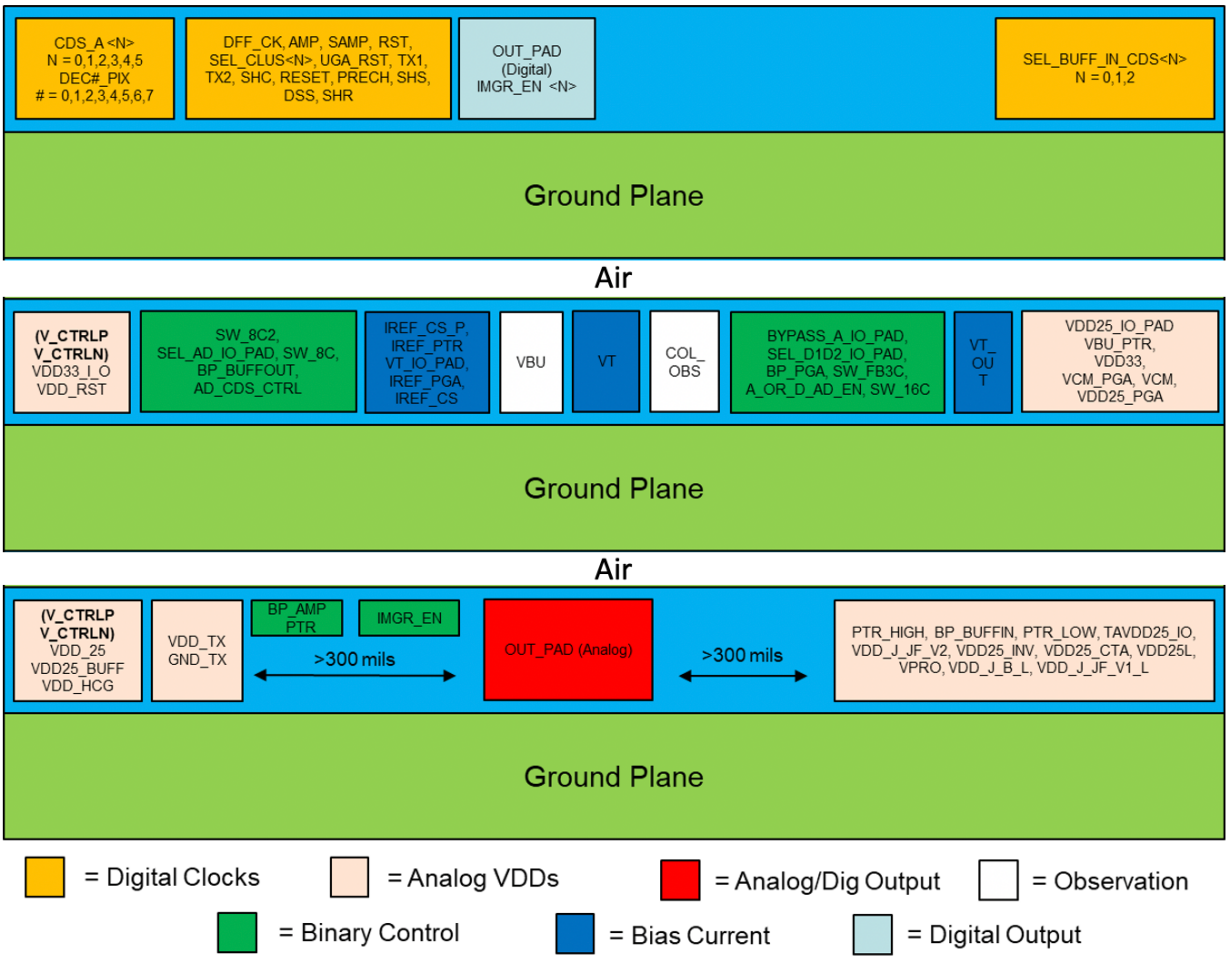

Figure 12: Signal layout for the flex section of the rigid-flex PCB. Diagram courtesy of Justin Gallagher.

Many sensitive analog and digital signals must traverse the rigid-flex cable to control QIS and transmit data. The layout of the flex sections was designed to mitigate noise on these signals. As shown in Figure 12, the traces were grouped by signal type and placed accordingly. Figure 12 represents the layer stackup of the flex sections and provides a cross-sectional view of the trace grouping. The spacing of the traces was selected to minimize crosstalk. The noise simulations were performed by staff researcher Justin Gallagher using equivalent circuits with SPICE software.

3.5 Discussion

This work provided insight into the design of the supporting hardware of sensitive imaging devices. The specific design challenges of this application motivated a thorough analysis of necessary changes and possible performance improvements over the initial Dartmouth design. The analysis of the grounding and power supply systems provided a deeper understanding of the system for the team for more effective design and use. The analysis and design work completed for this supplemental project aided in preparing for manufacturing and testing the system. Currently, the entire system has been manufactured and assembled.

Possible future improvements could come in many forms. The system could be simplified to the use of a single power supply. As discussed above, this improvement could reduce noise and simplify the system for easier debugging. Additionally, the data transmission could be replaced with optical lines to improve isolation between the CEB and the FPGA.

The NASA SAT-funded project provided excellent experience in sensitive electronics design. Hopefully, the details and recommendations identified during this project will continue to help with the smooth design of new systems.

4 Pinned Photodiode Simulation

This section includes the simulation of a 2D Indium-Gallium-Arsenide (InGaAs) pinned photodiode in Synopsis Sentaurus TCAD. The Sentaurus project was created by post-doctoral researcher George Nelson, Ph.D., to investigate the performance of an InGaAs photodiode in photon counting applications. This report describes the addition of a transient simulation profile to the existing project. The temporal profile enables the observation of the operation of the photodiode in time and enables control of the transfer gate. Additionally, this section includes a brief discussion of the definition of dark current in active pixel sensors (APS).

4.1 Simulation Setup

A 2D pinned photodiode structure without readout circuitry was simulated in Synopsis Sentaurus TCAD. To simulate a device in Sentaurus, a Sentaurus Workbench project must be created. Sentaurus Workbench is the main graphical interface for the suite of simulation tools which is used to manage a grouping of scenarios that follow a similar structure. Each scenario follows a predetermined path through a range of simulation tools.

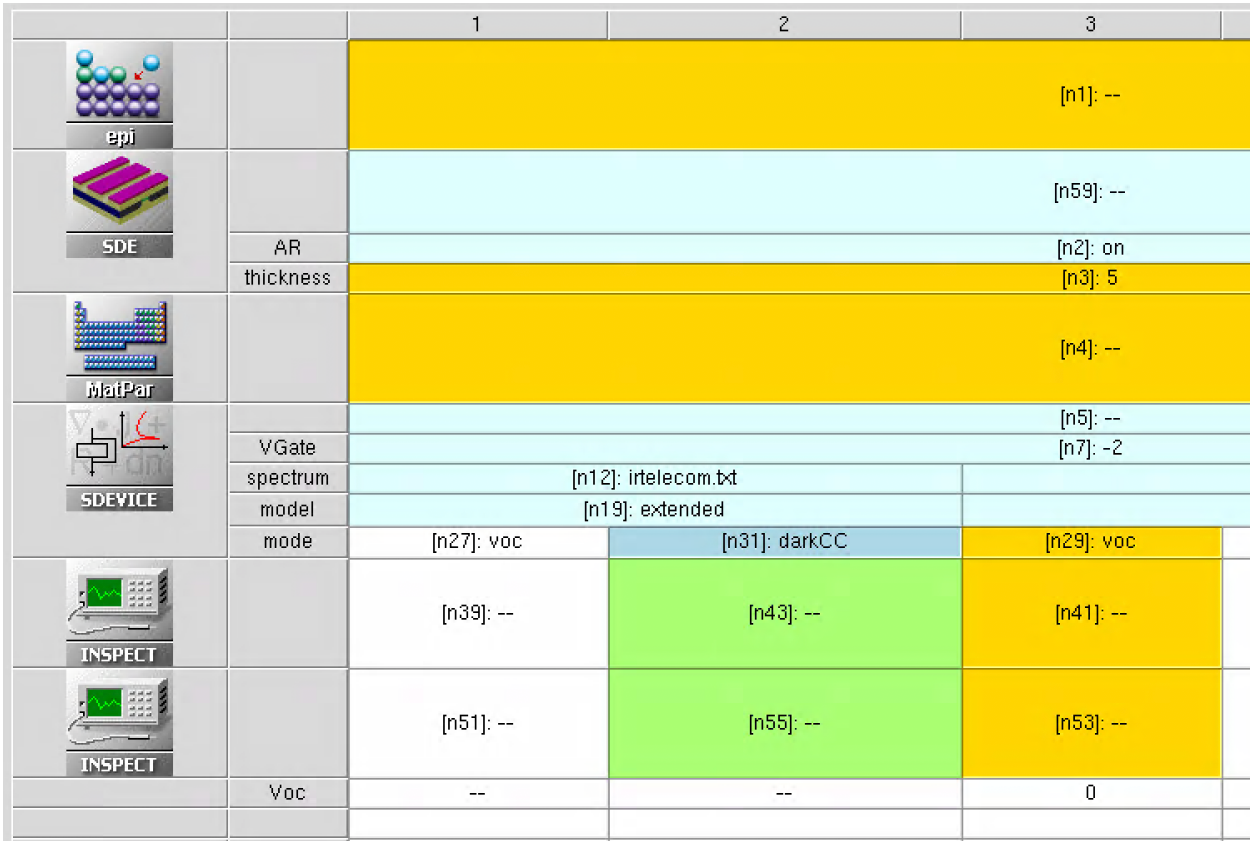

Figure 13: A partial view of the Sentaurus Workbench user interface.

In the case of this project, the simulation uses the following tools: Epi, SDE, MatPar, SDevice, and inspect. This flow is shown on the left side of Figure 13, and this report pertains to work done within the SDevice tool. Sentarus Device (SDevice) is a tool that manages the simulation of a semiconductor device by various means. The tools prior to SDevice exist to estimate the manufacturing process and prepare the device structure for simulation. The simulated optical input for these experiments was a 0.5 μm wide beam of 1550 nm light aligned with the center of the storage well with an intensity of 0.1 W/m^2, and the device was top-side illuminated.

4.2 Photodiode Design

The photodiode is a 2D model of a pinned photodiode without any readout circuitry. The photodiode was designed by Dr. Nelson of the Nanopower lab at RIT. The photodiode is constructed as shown in Figure 14. As mentioned above, no readout circuitry was included. Within the transient simulation, external voltages are applied to mimic readout circuitry. The photodiode is made up of a few main regions: the substrate, storage well, floating diffusion, gate, and anti-reflective coating. The standard photodiode design is described in more detail in the introduction section.

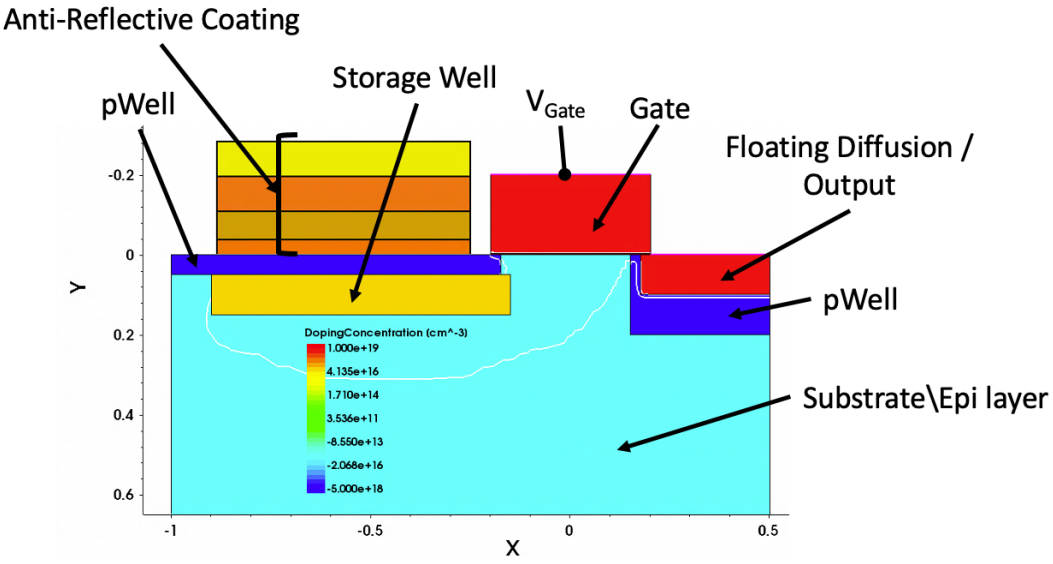

Figure 14: Labeled photodiode structure with doping concentration from Sentaurus Visual.

In this simulation, an anti-reflective (AR) coating was implemented. The coating helps capture more signal by reducing the refractive index step between air and the semiconductor material. Air and InGaAs have refractive indices of approximately 1 and 8.9, respectively. The large and abrupt gap between the two regions causes large amounts of reflections, ultimately

reducing the possible signal captured and total quantum efficiency. The AR coating reduces this gap with multiple layers with intermediate refractive indices.

4.3 Simulation Description

This section describes the various simulation profiles created within Sentarus Device (SDevice). Simulations are run on a server in the NanoPower Research Lab (NPRL).

4.3.1 Open Circuit Voltage Simulation

The open-circuit voltage (VOC) simulation profile was written by Dr. Nelson. If the gate is open and photoelectrons can flow to the floating diffusion (FD), the voltage measured from the FD to the substrate indicates the instantaneous photovoltage. Figure 15 represents the voltage measurement performed for the VOC profile.

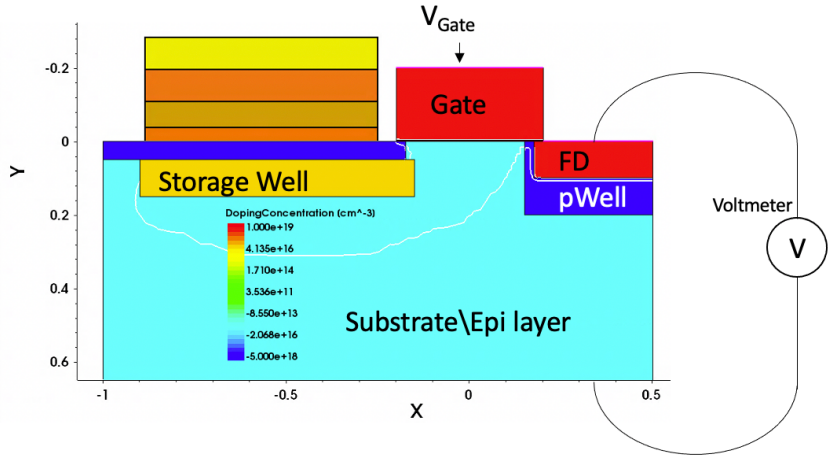

Figure 15: The measurement performed in the open-circuit voltage simulation profile is a voltage reading from the floating diffusion to the substrate. Courtesy of Dr. Nelson.

4.3.2 Transient Simulation

The transient function in Sentaurus Device was used to create time-dependent results. The transfer gate is controlled by assigning a preset voltage at specified time steps during the simulation. The gate control methodology is adapted from a Sentarus example project [28]. At the start of the SDevice file, sampling times are defined, and these timestamps are used to assign voltages to the gate within the electrode section of the SDevice file. The code for this implementation is described in Figure 16. Figure 17 demonstrates the results of this profile, showing the changing voltage on the gate over time as they correspond with the time step definitions in Figure 16.

Two pulses of the transfer gate were defined. The variables `_t1_` and `_t2_` , or t_1 and t_2, define the midpoints of each pulse. The following variables t_{1a} , t_{1b} , t_{1c} , and t_{1d} were algorithmically calculated based on the pulse midpoints. These calculations are based on t_b, the desired pulse width, and δt, the rise time. Additionally, pulse voltage levels $V_{p\ min}$ and $V_{p\ max}$ are the desired 'off' and 'on' states of the transfer gate, respectively.

```
#-- Voltage Levels
#define _vpmin_    2.0
#define _vpmax_    -2.0

#-- Sampling Times for Gate Voltage
#define _tb_       2.0e-5
#define _dt_       1e-5

#define _t1_       2e-5
#define _t2_       @<_t1_+ 10e-5>@

#define _t1a_      @<_t1_ - _tb_/2 - _dt_>@
#define _t1b_      @<_t1_ - _tb_/2>@
#define _t1c_      @<_t1_ + _tb_/2>@
#define _t1d_      @<_t1_ + _tb_/2 + _dt_>@

#define _t2a_      @<_t2_ - _tb_/2 - _dt_>@
#define _t2b_      @<_t2_ - _tb_/2>@
#define _t2c_      @<_t2_ + _tb_/2>@
#define _t2d_      @<_t2_ + _tb_/2 + _dt_>@
```



```
Electrode {

  ...

  { Name= "substrate"  Voltage = 0.0}

    *two pulses
    { Name= "gate"  Voltage= _vpmin_
         voltage=( _vpmin_ at _t1a_, _vpmax_ at _t1b_,
                   _vpmax_ at _t1c_, _vpmin_ at _t1d_,
                   _vpmin_ at _t2a_, _vpmax_ at _t2b_,
                   _vpmax_ at _t2c_, _vpmin_ at _t2d_ )}

  ...

}
```

Figure 16: These code sections describe the process for controlling the gate voltage in time. The top section shows the definition of the gate control timesteps and corresponds with Figure 17. The second section describes the application of the timesteps in the electrode section of the SDevice file.

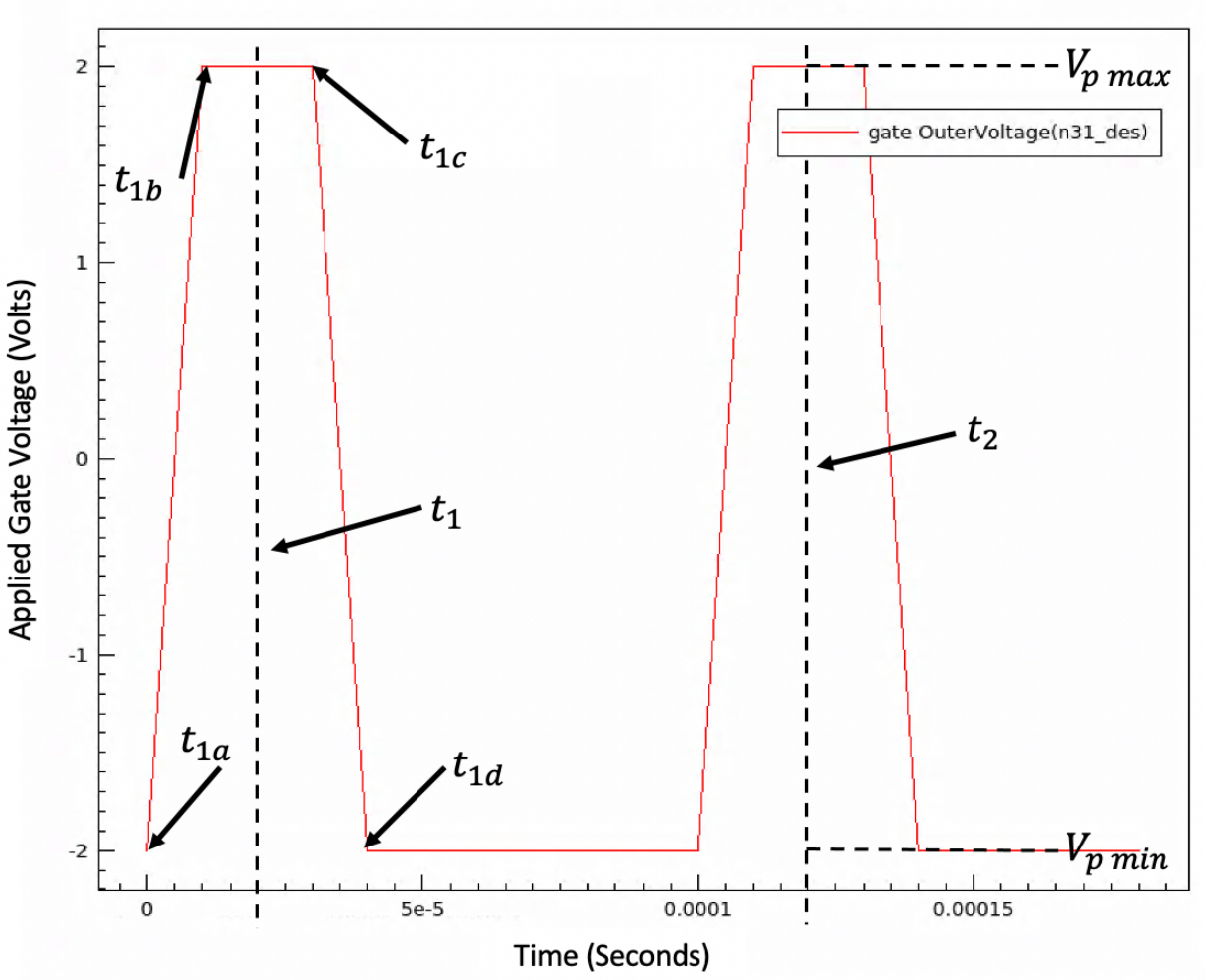

Figure 17: Plot of changing gate voltage versus time during a transient simulation.

4.3.3 Dark Current Simulation (Future Work)

In this experiment, dark current is defined as the phenomenon in which charge generated without incident light is moved into the storage well where it accumulates. Some also charge accumulates in the FD in the same way. However, the dark charge in the FD is removed prior to measurement by resetting the FD before transferring charge from the storage well. The described timing is shown in Figure 4. In this setting, dark current is measured by performing a standard capture as described earlier. Using the transient simulation technique, the gate can be enabled and

disabled to empty the storage well before the integration and to transfer charge after the integration. In order to operate the device without readout circuitry, the floating diffusion must be reset prior to the activation of the transfer gate. Unfortunately, during this project, a method to accomplish this was not identified.

4.4 Discussion

This project provided helpful insight into the processes and challenges of photonic device simulation. The initial goal of this work was to create a complete simulation of an InGaAs photodiode over the course of one academic year as a proof of concept for a future project. In this regard, the project was partly successful. Progress towards this goal was made in the form of the implementation of time-based simulation and the clarification of relevant terms for this use case. Within the constraints faced, it is hoped that the somewhat limited results are useful and can help guide further investigations.

5 Conclusion

This report demonstrates that the two projects incorporated in this MS paper provided an excellent overview of the many stages of development of next-generation solid-state imagers. The faculty, post-doctoral researchers, and research assistants involved in this work provided examples of excellent research practices and responsible approaches to experimentation. Further, the multi-faceted approach to this research created a great deal of interest for the author in solid-state imager research.

The NASA SAT-funded project provided insight into the practical aspects of camera design. Once imagers are fabricated, supporting hardware must be developed to power, control, and interact with them. With modern, complex imagers, this is not a simple task. This report describes work provided to a long-term project the has involved many researchers. The contributions primarily included an analysis of the grounding and power scheme of the camera system and resulting design recommendations.

Further, the photodiode simulation project provided an introduction to TCAD for photonics. An InGaAs pinned photodiode was simulated with the goal of measuring dark current. While this goal was not achieved, progress was made that can be used by future researchers.

This report serves to fulfill the requirement of the MS project for the MS degree in electrical engineering at RIT. The work detailed in this report meets the goal of the MS project to provide deeper experience in a subfield of electrical engineering to MS students. This project is the combination of two semesters of work on two separate projects within the same lab.

6 Appendix A – Tutorials

The purpose of this section is to provide information for those interested in working with software packages used in this report. The links included are working at the time of writing.

Company	Software	Tutorial
Autodesk	Eagle	The EAGLE Schematic & PCB Layout Editor - A Guide
https://intranet.ee.ic.ac.uk/t.clarke/EAGLE/The%20EAGLE%20Guide.pdf		
Synopsis	Sentaurus	A Primer on TCAD
http://www.micro.deis.unibo.it/~rudan/MATERIALE_DIDATTICO/diapositive/TCAD/04_TCAD_laboratory_diode_GBB_20140402H1246.pdf		
Starnet	FastX	Using FastX
https://www.rit.edu/researchcomputing/instructions/Using-FastX		
RIT VPN	Cisco AnyConnect	Virtual Private Network
https://www.rit.edu/its/services/network-communication/vpn		
Microsoft	Remote Desktop	Remote Desktop Gateway
https://www.rit.edu/its/services/helpful-resources/remote-desktop-gateway		

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